17 Gb/s VCSEL Driver Using Double-Pulse Asymmetric Emphasis Technique in 90-nm CMOS for Optical Interconnection

Kenichi Ohhata, Hironori Imamura, Toshinobu Ohno, Takaya Taniguchi, Kiichi Yamashita
Dept. of Electrical and Electronics Engineering
Kagoshima University
Kagoshima, Japan
k-ohhata@eee.kagoshima-u.ac.jp

Toru Yazaki, Norio Chujo
Production Engineering Research Laboratory
Hitachi, Ltd.
Yokohama, Japan

Abstract—This paper describes the design and experimental results of a 17 Gb/s vertical-cavity surface-emitting laser (VCSEL) driver using a double-pulse asymmetric emphasis technique. In this technique, the first pulse compensates for the parasitic capacitances and the second pulse compensates for the ringing, which enables a good eye opening even when the data rate increases. A test chip fabricated using a 90-nm CMOS technology generates a clearly open optical eye at a data rate of 17 Gb/s, which is approximately twice the VCSEL bandwidth.

I. INTRODUCTION

Recently, the demand for high-speed data transmission between LSIs on circuit boards in high-performance computers and router systems has increased. Thus far, electrical interconnections have been employed for data transmission between LSIs on a board; however, the transmission loss due to conductive and dielectric losses increases with the data rate. This limits the data rate and transmission distance in an electrical interconnection.

Optical interconnection, in which an optical waveguide is employed instead of a metal line, has attracted considerable attention as a promising solution to this problem. Many studies have focused on developing high-speed, low-power transceivers for optical interconnection [1–7]. The loss of the waveguide is significantly lower than that of the metal line; therefore, high-speed data transmissions that exceed the metal line transmission limit can be achieved. However, optical waveform degradation becomes a serious issue as the data rate increases because of parasitic capacitance and nonlinear response of the vertical-cavity surface-emitting laser (VCSEL). In some studies, a pre-emphasis technique incorporating a finite impulse response (FIR) filter used in the electrical interconnection was applied to the VCSEL transmitter in order to suppress waveform degradation due to the parasitic capacitance [4–6]. However, because the FIR filter is a linear system and the VCSEL response is nonlinear, this technique cannot suppress waveform degradation due to the nonlinear VCSEL response. The nonlinear effect of the VCSEL can be suppressed to some extent by increasing the average current when the extinction ratio is small. However, the nonlinear effect increases to such an extent that the FIR filter cannot suppress the waveform degradation when the extinction ratio is designed to be large in order to improve the receiver sensitivity. In order to solve this problem, we have proposed an asymmetric emphasis technique [7]. This technique can separately control the emphasis pulses at the rising and falling edges and can therefore suppress the nonlinear response of the VCSEL. The asymmetric emphasis technique effectively compensates for the nonlinear response; however, this technique cannot sufficiently compensate for the parasitic capacitance. Therefore, it is difficult to obtain an adequate eye opening using the asymmetric emphasis technique when the data rate increases.

In this paper, we begin by discussing the problem of the conventional asymmetric emphasis (CAE) technique; then, we propose a double-pulse asymmetric emphasis (DPAE) technique to solve this problem. Next, we discuss the effectiveness of the proposed technique from a quantitative perspective. Then, the construction and circuit techniques used in a VCSEL driver employing the proposed technique are described in detail. Finally, the experimental results of the fabricated VCSEL driver test chip are discussed.

II. DOUBLE-PULSE ASYMMETRIC EMPHASIS TECHNIQUE

A VCSEL driver modulates the optical output by changing the current flowing through the VCSEL (I_p), as shown in Fig. 1. When the modulation current waveform without emphasis is applied to the VCSEL, the relaxation oscillation generates ringing at the rising and falling edges of the optical waveform. This ringing considerably degrades the eye opening. Thus, we proposed an asymmetric emphasis technique to compensate for the ringing. In this technique, the height, width, and setup of the emphasis pulses are controlled separately at the rising and falling edges. We generate a positive emphasis pulse to
compensate for the undershoot at the rising edge and a negative emphasis pulse to compensate for the overshoot at the falling edge. The width and setup time of each emphasis pulse were adjusted according to both the undershoot and the overshoot. This adjustment tends to suppress the ringing due to the nonlinear response of the VCSEL.

However, when the data rate increases, the waveform degradation of intersymbol interference (ISI) due to the parasitic capacitances ($C_p$ and $C_{VC}$) becomes dominant. The CAE technique can compensate for the parasitic capacitances by setting the setup time of the emphasis pulse to 0; however, in this case, the ringing due to the nonlinear response cannot be compensated. Thus, the CAE technique cannot deal with both the ISI due to the parasitic capacitances and the ringing due to the nonlinear response because the timing and height of the emphasis pulse that compensates for the parasitic capacitances and ringing are quite different. To overcome this problem, we proposed the DPAE technique that generates the first pulse to compensate for the parasitic capacitances and the second pulse to compensate for the ringing. A good eye opening can be obtained by the DPAE technique even when the data rate increases.

Fig. 2 shows the calculated data rate dependence of the width and height of the eye opening. The VCSEL output eye pattern is calculated by using a rate-equation-based VCSEL model and the current pulse is applied to the VCSEL by an ideal current source. The bandwidth of the VCSEL at a bias current of 4 mA is approximately 9 GHz. The parasitic capacitance $C_p$ is 1 pF. The eye opening width in the conventional FIR-filter-based emphasis technique decreases with the data rate because the jitter increases as a result of the ringing. The eye opening height in the CAE technique decreases with the data rate because the ISI due to the parasitic capacitance increases. On the other hand, the DPAE technique maintains a good eye opening width and height up to 17 Gb/s, which is approximately twice the VCSEL bandwidth.

III. CIRCUIT IMPLEMENTATION

Fig. 3 shows the circuit configuration of a VCSEL driver employing the DPAE. This circuit comprises a modulation pulse generator (MPG), rising and falling emphasis pulse generators (REPG1, 2 and FEPG1, 2), and rising and falling edge detectors (RED and FED). The MPG generates a modulation current pulse according to the data signal $D$; this pulse is used to switch the VCSEL on or off. The RED detects the rising edge of $D$ and then reverses the output ($V_{RE}$). $V_{RE}$ is delayed by the two variable delayers in REPG1, and subsequently, $V_{RE11}$ and $V_{RE12}$ are generated. An XOR-gate current switch outputs the emphasis current pulse only when $V_{RE11}$ and $V_{RE12}$ differ from each other. The delays of $V_{RE11}$ and $V_{RE12}$ are controlled by the variable delayers; as a result, the delay and width of the emphasis pulse can be adjusted arbitrarily. REPG2 has the same construction as REPG1. In a...
similar manner, FEPG1 and FEPG2 generate emphasis pulses that are synchronized with the falling edge. FEPG1 and FEPG2 generate negative emphasis pulses because they output the current in the reverse direction by using a PMOS current mirror. Thus, the proposed circuit can generate a double-emphasis pulse. Moreover, the height, width, and setup time of the emphasis pulse can be adjusted arbitrarily.

Fig. 4 shows a schematic of the rising-edge detector. The circuit configuration is the same as that of a frequency divider; that is, the configuration comprises a master-slave latch whose output is fed back to the input. Whenever the data signal $D$ rises, the output of this circuit ($V_{RE}$) is reversed. The variable delay (Fig. 5(a)) comprises three CML buffers and a 4:1 selector. Fig. 5(b) shows a CML buffer with a cascode stage. The 4:1 selector comprises CML current switches with a disable function (Fig. 5(c)). The MOS transistor MCS operates as the current source if the control signal $SEL0$ is “1,” and the MCS cuts off if the $SEL0$ is “0.” The current switch can be enabled or disabled by the control signal. One of the four current switches is enabled, and the selected signal ($IN0$ to $IN3$) is outputted. The number of buffer stages can be changed by the selector to allow delay adjustment.
IV. EXPERIMENTAL RESULTS

A test chip of the VCSEL driver was fabricated by using a 90-nm CMOS process (Fig. 6). The driver-circuit core area was $220 \times 330 \mu m$. The supply voltage was 1 V, and the power dissipation of the driver was 150 mW/ch. The driver chip and an array of four VCSELs were connected by wire bonding. The wavelength and bandwidth of the VCSEL were 850 nm and 9 GHz at the bias current of 4 mA, respectively. Examples of electrical output waveforms are shown in Fig. 7. The waveforms are measured by using an RF probe. The height, width, and setup time of the emphasis pulse can be controlled and a double-emphasis pulse can be observed. The optical eye patterns at data rates of 15 and 17 Gb/s are shown in Fig. 8. The output optical signal from the VCSEL was received by a light-wave probe made of multimode fiber and was input to a photo detector. The output signal of the photo detector was amplified using a broadband amplifier, and the waveform was observed using an oscilloscope. A clear eye opening could be obtained at 17 Gb/s, which is approximately twice the VCSEL bandwidth. This driver was designed to prove the effectiveness of the double-pulse asymmetric emphasis technique. In this context, we believe that future studies should focus on decreasing the power dissipation of the driver. We have already begun work on an improved design. In this design, the power dissipation is expected to be reduced to half of that in the current design because most circuits comprising an emphasis pulse generator will be replaced by CMOS logic circuits.

V. CONCLUSION

We have proposed a double-pulse asymmetric emphasis technique that generates the first pulse to compensate for the parasitic capacitances and the second pulse to compensate for ringing; this ensures a good eye opening even when the data rate increases. A test chip fabricated using 90-nm CMOS technology generated a clearly open optical eye at a data rate of 17 Gb/s.

REFERENCES


