Dithering Skip Modulator with a Width Controller for Ultra-wide-load High-Efficiency DC-DC Converters

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Abstract—This paper proposes a temperature-independent load sensor to decide the optimum power MOSFET width for power saving of DC-DC converters. Besides, it also can decide the optimum modulation technique in tri-mode operation, which is composed of pulse-width modulation (PWM), pulse-frequency modulation (PFM), and a new proposed dithering skip modulation (DSM). An efficiency-improving DSM operation is introduced to raise the efficiency drop because of transition from PWM to PFM. Importantly, DSM mode can dynamically skip the number of gate driving pulses, which is inverse proportional to load current. Simplistically, and qualitatively stated, the novel load sensor can automatically select the optimum modulation method and optimum power MOSFET width to achieve high efficiency over a wide load range. Experimental results show the tri-mode operation can have high efficiency about 89% over a wide load current range from 3mA to 500mA. Owing to the effective mitigation of the switching loss contributed by large power MOSFET, the novel width controller not only achieves high efficiency about 95% but also extends this high efficiency to a lower load current range about 0.1mA.

I. INTRODUCTION

As we know, a popular technique to improve the efficiency over a wide load range is the hybrid mode, which is composed of pulse-width modulation (PWM) and pulse-frequency modulation (PFM) [1-2]. Hybrid mode achieves a high efficiency for the load current region A and B in Fig. 1. However, there exists an efficiency dropping in region C. It means that the efficiency curve is not smooth at the transition between PWM mode and PFM mode. It is a matter of efficiency and current load range for hybrid-mode modulation technique. The hybrid-mode modulation can maintain a high efficiency by closing the two peak efficiency values to reduce the efficiency drop at the sacrifice of load range. Therefore, a dithering skip modulator is proposed to raise the efficiency between PWM and PFM curves in Fig. 1. In other words, the efficiency drop between PWM and PFM modes can be raised by the novel DSM mode.

Besides, a novel temperature-independent load sensor is also proposed to dynamically switch among these three modes, which are PWM, PFM, and DSM modes. Furthermore, compared with pulse-skipping mode and burst mode [3-5], DSM mode uses the dithering technique to reduce the output ripple [6]. Due to the insertion of DSM mode, a wide load range and high efficiency can be achieved by the insertion of DSM mode without sacrificing the load range of conventional hybrid mode. Without increasing output voltage ripple, the improved result is expected as the smooth efficiency curve from PWM mode curve to DSM mode curve and further extending to PFM mode.

One prevailing technique called dynamic adjustment for the width of the power MOSFET transistors can have the same advantage of improving efficiency as that of changing modulation technique in tri-mode operation. By combining dynamic adjustment width control technique with load sensor, the optimum width of power MOSFET and small size driver can be chosen to save much power. Therefore, the dash line in Fig. 1 shows the efficiency of the tri-mode buck DC-DC converter with the width controller. Obviously, the width controller can raise the efficiency to about 95%. Beside, compared with the conventional design without width controller, the efficiency can be raised to a higher value in case of very light load because the width is kept a reasonable small size by the width controller. In other words, the high efficiency performance in PFM operation can be extended to very light load.
load in region D. The ultra-wide-load high-efficiency is achieved by tri-mode operation with width controller.

II. ARCHITECTURE OF BUCK DC-DC CONVERTER

In Fig. 2, the buck DC-DC converter is modulated by a tri-mode controller, which is composed of PWM, PFM, and DSM modes. A temperature-independent load sensor estimates the load condition and sends the digital decision codes \(D_1, D_2, \ldots, D_N\) to decoder in order to dynamically select one optimum modulator from the three modules. Compared with the prior design [1], the buck DC-DC converter does not need an external pin to decide the optimum modulator.

The load sensing technique utilizes the prior literature [7], which is called SENSEFET topology. During the sensing period, the P-type power MOSFET is turned on by setting signal \(SW_P\) low and the sensing current \(I_{sense}\) is equal to a \(N\)-th of inductor current \(I_L\). \(N\) is an integral number. By the sensing resistor \(R_{sense}\), the sensing current can be transferred to a sensing voltage \(V_{sense}\). However, even though \(V_{sense}\) is direct proportional to the load current, it is difficult for simple comparators to decide the switching points of three controllers because the change of \(V_{sense}\) is too small.

Thus, a temperature-independent load sensor, which is composed of a sample-and-hold circuit, a V-I converter and a current-mode delay-line A/D converter is proposed to determine the load condition as shown in Fig. 3. At first, sensing voltage \(V_{sense}\) is sampled and held to get a peak voltage by \(clk_{sam}\) signal. In order to avoid unnecessary mode switching and save the power consumption, the sensing clock \(clk_{sam}\) is periodically generated for several times of switching cycles and is inverted to generate the active-low resetting pulse \(V_{reset}\) to reset each delay cell simultaneously in the delay-line chain. Besides, the V-I converter [8] converts the peak value of \(V_{sense}\) to a current signal for driving the delay-line A/D converter, owing to the characteristic of subtracting \(I_{ds}\) from \(I_{ds}\), the temperature independent current \(I_{ds}\) is written as:

\[
I_{ds} = I_{ds1} - I_{ds2} = \frac{V_{sense}}{R_s} = \frac{I_L}{N} R_{sense} R_s
\]

With the current mirror structure, the delay-line A/D converter is also independent of temperature variation.

The concept of DSM mode is illustrated in Fig. 4. Due to DS period is determined by two signals \(V_{mod}\) and \(I_L\), the decreasing load current increases the size of DS period as shown in Fig. 4 (a) to (c). In other words, the size of DS period is inversely proportional to the load current. Thus, a DS period gradually contains more DS modules when the load current continuously decreases. In order to reduce the output voltage ripple and the switching consumption of power MOSFET, the dithering skip pulse signal is generated by DS modules. The function of a DS module is to make the DC-DC converter skip one switching pulse among three continuous switching cycles. Certainly, much power can be retrenched when load current reduces gradually. Besides, if the ultra-powerless is turned on, each DS module is composed of one ON signal and two OFF signals to get more skipping pulses.

Fig. 3. Schematic of the current-mode delay-line A/D converter.

Fig. 4. Timing diagrams for dithering skip modulator. (The values of load current are: (a) > (b) > (c) )

Fig. 5. The timing waveforms of delay-line chain and \((D_1, D_2, D_3) = (1, 1, 0)\) at pulse trigger.
An example of the timing diagram generated by the delay-line chain is shown in Fig. 5. A periodic pulse \( V_{mode} \) triggers the register in the load sensor to latch the outputs of the delay-line chain. In order to increase the total delay time in DSM mode, extra delay cells can be added to the delay-line chain. Therefore, the signals \( (t_1 - t_0) \) do not need to switch from consecutive delay cells. And the choice of \( t_i \) is a trade-off between efficiency and output voltage ripple in DSM mode. Hence, the output of delay-line A/D converter is decoded by the mode decoder to generate two mode-selected signals VPWM and VPFM. These two bits can select one optimum modulator from the three modulators. Table I shows the codes for determine the operation mode.

In Fig. 6, three digital mode bits \( (M_1, M_2, M_3) \) are selected from the digital word \( (D_0, D_1, ..., D_6) \). The selection of digital mode bits defines the sizes of three mode regions. The Boolean function of mode signals VPWM and VPFM are written as:

\[
\begin{align*}
V_{PWM} &= M_1 M_2 M_3 + M_2 (PWM)_{i-1} \\
V_{PFM} &= PFM_{end} \left( M_1 M_2 M_3 + (PWM)_{i-1} \right)
\end{align*}
\]

VPWM and VPFM are the current situation of load current, and VPWM\(_{i-1}\) and VPFM\(_{i-1}\) are the previous situation of load current. It is worth noting that a hysteretic region is needed between PWM and DSM mode to avoid unnecessary mode switching. Therefore, if PWM mode changes to DSM mode, the load current must be lower than \( I_{L2} \). Similarly, load current must be higher than \( I_{L3} \) to make control mode coming back to PWM mode. However, owing to PFM mode is operated in the discontinuous conduction mode (DCM), the peak value of \( V_{sense} \) can not be indicative of the average load current. Thus, the delay-line A/D converter will be reset and adopt a comparator named as ‘comp3’ to end the PFM mode when the load condition is heavy. In Fig. 6, a lower threshold voltage \( V_0 \) is set to determine whether the PFM mode can supply the output loading or not. Furthermore, the PFM mode is switched to PWM mode not DSM mode in order to supply much energy to reduce the output voltage ripple.

### Table I: Controller Mode Table

<table>
<thead>
<tr>
<th>Mode</th>
<th>VPWM</th>
<th>VPFM</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>DSM</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>PFM</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Scaling down the power MOSFET width can save much power dissipation in switching loss when the load condition is light. Oppositely, scaling up the power MOSFET width can save much power dissipation in conduction when the load condition is heavy. Besides, there does not need the large driver to charge or discharge the gate of power MOSFET. Because the new proposed width controller partitions the large power MOSFET into small power MOSFET units as shown in Fig. 8, each small power MOSFET unit has its own small tapering factor \( (a_i, b_i) \). In our design, \( a = 10.68, a_i = (a/12)^{0.66} = 4.66, \) and \( b_i = (a/6)^{0.66} = 5.88. \) As a result, the width of power MOSFET varies according to the loading condition; meanwhile, the driver for charging or discharging the gate of power MOSFET is changing with the optimum width. Owing to the variation of power MOSFET width, the efficiency curve...
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