A 10Gbps/port 8x8 Shared Bus Switch with embedded DRAM Hierarchical Output Buffer

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Abstract
A hierarchical buffering technique with the embedded DRAM (eDRAM) as a packet buffer is proposed for 10Gbps/port 8x8 shared bus switch. A prototype chip with 8 input ports and an output port is implemented by 0.16μm DRAM technology. To satisfy the required buffering capacity and memory bandwidth of 90Gbps, a 200MHz 32kb SRAM and four 25MHz 1Mb eDRAM macros are used hierarchically with 512bit interface. The die area is 13.8mm² including SRAM and DRAM.

1. Introduction
The output queueing switch has been accepted as an ideal switch in terms of performance, because it can provide maximized throughput as well as Quality of Service (QoS) (1). And, a shared bus switch, which is one type of the output queueing switches, has been widely used in many commercial switches and routers. In a conventional shared bus switch, each output line card is connected to a shared backplane on a board level (2). However, as the port speed increases up to 10Gbps, the concentrated bandwidth on the shared bus and output buffers become to bottleneck of the performance of the switch. The only way to overcome the bandwidth limitation is to integrate the switch system on the same chip.

The most challenging issue in on-chip shared bus switch is the output buffer design. It must support sufficient bandwidth to satisfy performance requirement while providing enough capacity to provide sophisticated QoS. Memories can be used as the output buffer. SRAM satisfies the bandwidth requirement but occupies large die area, and DRAM provides sufficient capacity but suffers from long latency.

In this work, we propose a hierarchical output buffering (HOB) technique to use only the advantages of the SRAM and the embedded DRAM (eDRAM) hierarchically in a pipeline (3) and a technique to doubling the I/O width of eDRAM macros to satisfy both of the bandwidth and capacity requirements. A prototype chip of HOB with eight input ports and one output port of 10Gbps per port is implemented and measured. In this paper, its implementation and the measured results will be explained in detail.

2. Hierarchical Output Buffering Technique
The required peak bandwidth of the output buffer is 90Gbps for input data in a 8x8 shared bus switch with the port speed of 10Gbps (Fig. 1). However, the average bandwidth is smaller than 10Gbps, otherwise the packet buffer will overflow immediately. The peak bandwidth appears only at hot spot situation when many input packets destine to an output port at the same time, a situation so called output conflict. In a HOB switch,
because the hot spot situation does not occur frequently due to a flow control mechanism, we prepared small capacity SRAM at the front of main packet buffer (Fig. 2).

All arriving packets, whose traffic pattern is irregular with peak bandwidth of 80Gbps, are buffered in SRAM, and then transferred to eDRAM with more regulated pattern. In this architecture, the fast dual-port SRAM is used for an instant peak bandwidth of 80Gbps and the eDRAM is for fulfilling the required large capacity.

The number of eDRAM macros, K, and the capacity of SRAM and eDRAM can be determined by the tradeoff between area cost and the switch performance such as packet loss probability or packet latency (3). To obtain optimal set of (K, SRAM capacity, DRAM capacity), we simulated various sets of configurations under the constraints of a packet loss probability less than 10^-6 and packet delay less than 4.8μsec at 90% offered load of the real Internet Protocol packet traffic. As the simulation results show, the set of (3, 32kb, 1Mb) shows least product of area cost and packet loss probability (See fig. 3). The implemented HOB switch has the same buffer size and architecture as the simulated optimal set [3].

3. Implementation of HOB

Packets are assumed to be composed of 512bit-size cells. The I/O bit-width of each memory in HOB switch is the same as the packet size. Fig. 4 shows a block diagram of the HOB with 8 input ports. PLL generates and synchronizes multiple clock sources such as 200MHz for SRAM and 25MHz for eDRAM macros. The 200MHz dual port SRAM has one write and one read port with 512bits interface. Each port guarantees the 80Gbps input bandwidth and 30Gbps output bandwidth (Fig. 5). The input traffic is generated from the embedded ROM to emulate 8 input ports with 10Gbps per port.

**Dual I/O scheme of eDRAM**

In traditional eDRAM macros, I/O circuits are placed in only one side because the I/O bit-width is much smaller than a page length. In the HOB switch, I/O interfaces of eDRAM macro are located on both of the up and down sides doubling I/O width into 512bits as shown in Fig. 6. The I/O interface lines constitute two 256b-wide S-D buses (SRAM to DRAM bus), through which SRAM transacts the cell data to eDRAM. By using the proposed dual I/O scheme, a cell data can be read or written in a single clock cycle. And this scheme is also optimal in terms of energy efficiency because the word size and the page size of eDRAM are matched with the packet size. To overcome the limited layout pitch, a Data Bus Sense Amplifier (DBSA) and a Write Driver (WDRV) are laid out per two Bit-Line Sense Amplifier (BLSA), and read/write of burst length 2 is supported with 2:1 MUX and DEMUX.

The fabricated chip photograph is shown in Fig. 7. It used 0.16um DRAM technology and 0.28um CMOS logic technology with 1 poly and three metal layers (1W+2Als).
The area of HOB switch including SRAM, S-D bus and eDRAM macros is 5.3mm x 2.6mm.

The test chip is wire bonded on a PCB board for measurement. The measured waveforms are shown in Fig. 8. 25MHz system clock is generated by PLL. Packets generated by four ROM are transacted through S-D buses at 200MHz frequency, and then come out to the output port after buffered in eDRAM for a while.

4. Conclusion

A hierarchical buffering technique to use embedded DRAM (eDRAM) as a packet buffer in 10Gbps/port 8x8 shared bus switch was proposed. A prototype chip was implemented and by 0.16um DRAM based SoC technology and measured to show a full performance of 10Gbps. In this chip, 200MHz 32kb SRAM and 25MHz 1Mb eDRAM were used hierarchically with 512bit interface to satisfy the maximum required memory bandwidth of 90Gbps and sufficient buffering capacity. The I/O width of eDRAM was expanded into 512bits by using a proposed dual I/O scheme. It shows packet loss rate less than $10^{-6}$ and packet latency less than 4.8μsec. The fabricated chip was measured

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5. References


Fig. 6 Both Side I/O scheme of 512x512 eDRAM Macro

Fig. 7 Prototype chip microphotograph of HOB switch on board

Fig. 8 Measurement results