Performance Investigation on the Reconfigurable Si Nanowire Schottky Barrier Transistors

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Abstract

In this paper, the performance of the reconfigurable Si nanowire schottky barrier transistors (RFETs) is investigated with simulation method. In contrast to conventional Schottky barrier MOSFETs (SB-MOSFETs) and silicon nanowire transistors (Si-NWTs) with metal/silicide as source/drain, the separate two gates in RFETs are located at the two Schottky junctions. Our simulation results show the variable electric characteristics and working principle of the RFETs working as p-/n-type. The RFETs exhibit higher on/off current ratio compared with other Schottky transistors.

1. Introduction

Nowadays, integrated circuits are made up of complementary metal oxide semiconductor (CMOS) devices which depend on the combination of n- and p-FETs. However, these devices need exact control of doping and can't change the electrical characteristic. With low series resistance, little random dopant fluctuation effect and low thermal budget, Schottky barrier MOSFETs (SB-MOSFETs) and silicon nanowire transistors (SB-Si-NWTs) have gained tremendous attention for a long time [1-4]. However, the Schottky Barrier transistors suffer from their ambipolar nature which leads to lower on/off current ratio compared with conventional transistors [5, 6]. So it is important to study how to improve the on/off current ratio of the Schottky Barrier transistors. The reconfigurable Si nanowire Schottky barrier transistors (RFETs) are presented recently which show the variable electric characteristics and high on/off current ratio [7, 8].

The performance of RFETs is mainly investigated with simulation method in this paper. Our simulation results show the variable electric characteristics and working principle of the RFETs working as p-/n-type. The RFETs exhibit higher on/off current ratio compared with other Schottky transistors.

2. Simulation Method and Device Structure

In our work, the performance of SB-Si-NWTs and RFETs is simulated with 3D device simulator Synopsys Sentaurus TCAD tools. The drift diffusion transport within the Si region, thermionic emission and quantum mechanical tunneling at the Schottky junctions are used. The electric characteristics on the performance of SB-Si-NWTs and RFETs are mainly discussed.

The schematic structures of the SB-Si-NWTs and RFETs for the simulations are plotted in Figure 1(a, b), with default parameters given in Table 1. Compared with conventional SB-Si-NWTs with metal/silicide as source/drain, the separate two gates in RFETs are located at the two Schottky junctions: program gate (Vg2) is to select p-/n-type configuration, control gate (Vg1) is to control the injection of the desired carriers into the channel. The gate length Lg/Lg1/Lg2 is 30nm, the length between two gates (L) is 30nm, the nanowire radius R is set to be 8nm, and the equivalent gate dielectric thickness Tox is 1nm. Intrinsic SB-Si-NWTs are used in our simulations. The Source-Drain voltage Vds ranges from 0 to 0.8V, The Gate-Source voltage Vgs/Vg1/Vg2 ranges from 0 to 1.5V. Silicide Schottky barrier height (SBH) is chosen to be 0.9 eV (suggesting PtSi [6]) and 0.66eV (suggesting $NiSi_2$, the Fermi level of which aligns near the intrinsic Fermi level of Si [7]).

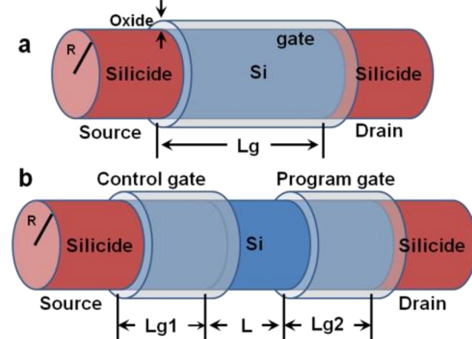

Figure 1. The schematic structures of (a) SB-Si-NWTs and (b) RFETs for the simulations

Table 1. Default parameters used in this work.

PARAMETERS	VALUES
Gate Length (Lg/Lg1/Lg2)	30 nm
Length between two gates (L)	30 nm
EOT(Tox)	1 nm
NWT Radius (R)	8 nm
Silicide Schottky barrier height (SBH)	0.9 eV, 0.66eV

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3. Results and discussions

The transfer curves and output curve of SB-Si-NWT when SBH=0.9eV and 0.66eV are simulated in Figure 2, 3. Figure 2 shows that the Schottky Barrier transistors suffer from their ambipolar nature which leads to lower on/off current ratio about 1×10^5 when Vds=−0.8V. The Drain Source voltage bias has much effect on the SB-Si-NWT, resulting in a shift of minimum drain-source current and lower on/off current ratio.

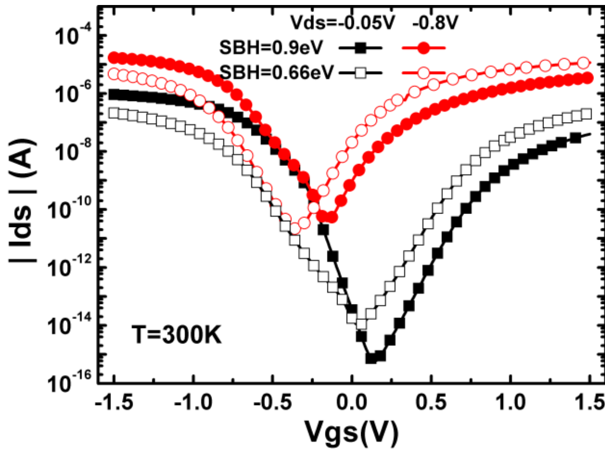

Figure 2. The transfer curves of SB-Si-NWT when SBH=0.9eV and 0.66eV

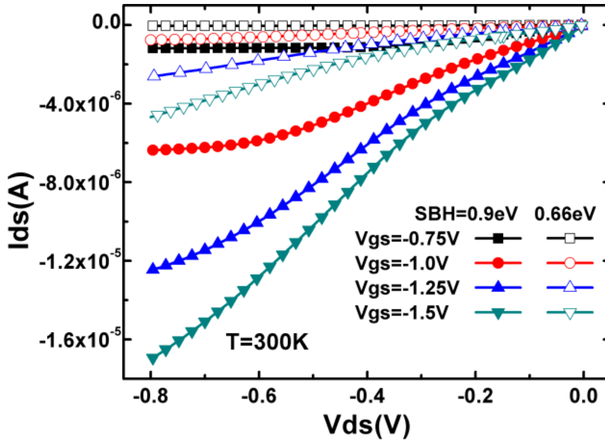

Figure 3. The output curve of SB-Si-NWT when SBH=0.9eV and 0.66eV

Figure 4 and 5 plotted the transfer curves and output curve of RFETs when SBH=0.66eV. Due to the separate two gates in RFETs located at the two Schottky junctions: one (Vg2) is to select p-/n-type configuration, the other (Vg1) is to control the injection of the desired carriers electrons/holes into the channel, the RFETs can achieve much lower off-state current and higher on/off current ratio about 1×10^{15}. Besides, the Drain Source voltage bias has little effect on the RFETs compared with SB-Si-NWT.

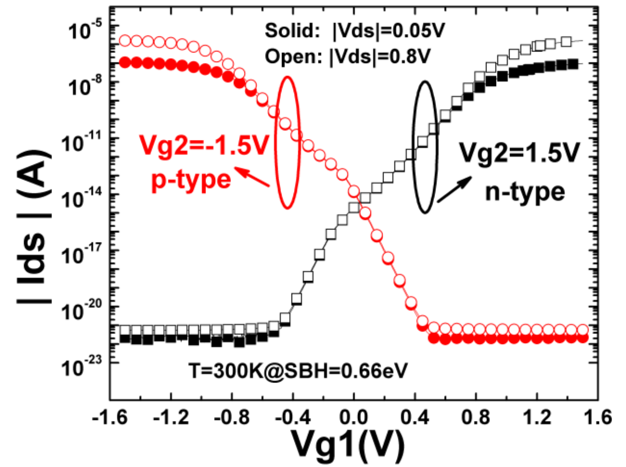

Figure 4. The transfer curves of RFETs when SBH=0.66eV

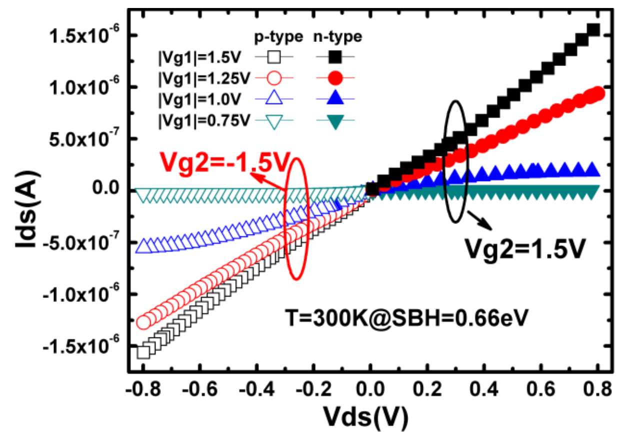

Figure 5. The output curve of RFETs when SBH=0.66eV

By calibrating the parameters, the transfer curves and output curve of SB-Si-NWT and RFETs in the simulation can be well consistent with the experimental data in [7, 9]. The RFETs can achieve much lower off-state current, while the on-state current is lower than SB-Si-NWTs due to the difference of the silicon nanowire length. RFETs exhibit high Ion/Ioff ratio of about 1×10^{15} compared with that of about 1×10^5 in SB-Si-NWTs. Besides the RFETs suffer little from the ambipolar nature and drain-source bias voltage which leads to high on/off current ratio compared with SB-Si-NWTs.

In order to better show the variable electric characteristics and working principle of the RFETs working as p-/n-type, we plot the band structure on the surface of Si Nanowire along the x-axis for the p-programmed on-state and off-state in Figure 6 and 7.

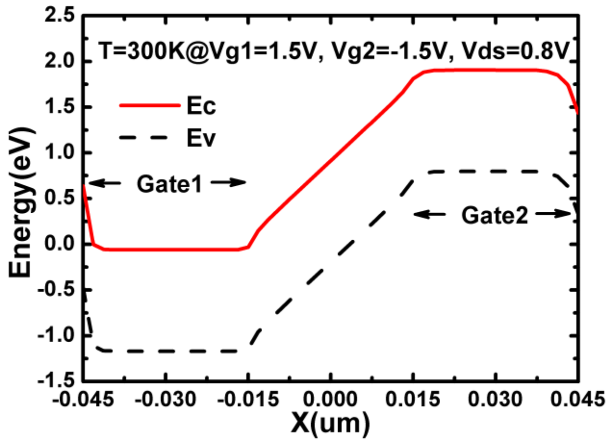

Figure 6. Band structure on the surface of Si Nanowire along the x-axis for the p-type off-state

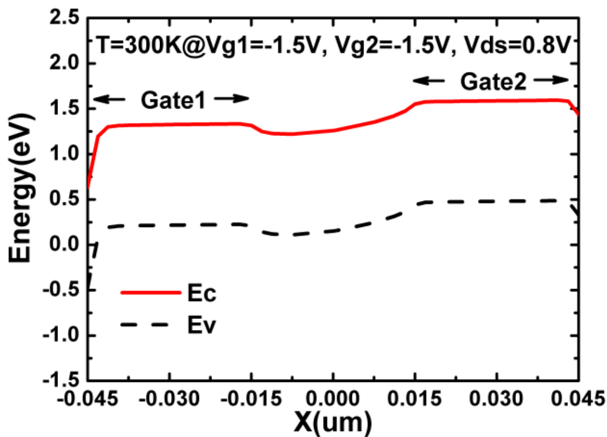

Figure 7. Band structure on the surface of Si Nanowire along the x-axis for the p-type on-state

The RFETs working as p-type are programmed by setting the program gate Vg2 to −1.5V (1.5V for n-type) and the drain-source voltage Vds to −0.8V (0.8V for n-type). The program gate Vg2 can effectively blocks electron/hole injection at the drain electrode and the control gate Vg1 is swept between positive and negative values. When Vg1=−1.5V, the upward bending of energy band structure stimulates hole injection into the active region at the source side. When Vg1 changes to positive values 1.5V, it blocks the injection of holes and reduces the drain-source current of the RFETs, which corresponds with Figure 4. The spacecharge density distribution of cross section along the x-axis for the p-type off-state and on-state are plotted in Figure 8. We can also get the variable electric characteristics and working principle of the RFETs working as n-type.

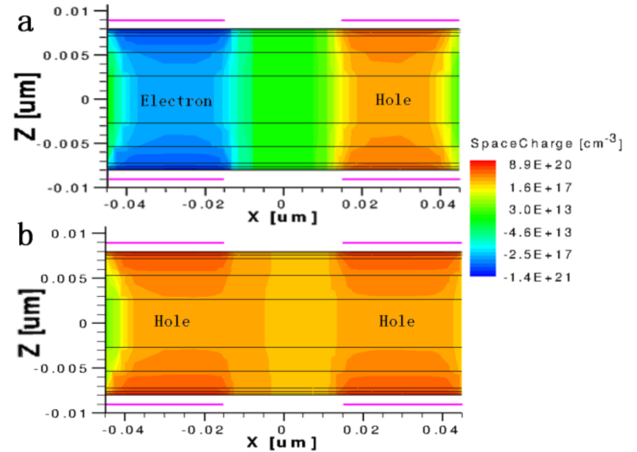

Figure 8. Spacecharge density distribution of cross section along the x-axis for the p-type (a) off-state and (b) on-state

4. Summary

The performance of RFETs is investigated with simulation method. In contrast to SB-Si-NWTs with metal/silicide as source/drain, the separate two gates in RFETs are located at the two Schottky junctions. Our simulation results show the variable electric characteristics and working principle of the RFETs working as p-/n-type. The RFETs exhibit higher on/off current ratio compared with SB-Si-NWTs and RFETs suffer little from the ambipolar nature and effect of drain-source bias voltage.

Acknowledgments

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