A Fully Integrated CMOS Clock Data Recovery IC for OC-192 Applications; J. Li, et.al.

Jinghua Li, Jose Silva-Martinez, Brian Brunn, Shahriar Rokhsaz, Moises E. Robinson

Abstract— In this paper, a fully integrated OC-192 clock-data recovery (CDR) architecture in standard 0.18μm CMOS is described. The proposed architecture integrates the typically large off-chip filter capacitor by using two feed-forward paths configuration to generate zero and pole and satisfies SONET jitter requirements with a total power dissipation (including the buffers) of 290mW. The measured RMS jitter of the recovered data is 0.74ps with a bit-error rate (BER) less than $10^{-12}$ when the input PRBS data pattern has a pattern length of $2^{15}-1$ and a total horizontal eye closure of 0.54 UI$_{pp}$ due to the added ISI distortion by passing data through 9 inches FR4 PCB trace. The chip exceeds SONET OC-192 jitter tolerance mask, and high frequency jitter tolerance is over 0.31 UI when applying PRBS data with a pattern length of $2^{15}-1$.

Index Terms— Clock and data recovery circuits, Monolithic CDRs, Full On-chip CDR, data communication circuits, OC-192, SONET, phase-locked loops.

I. INTRODUCTION

Demands for low cost transceiver IC have been boosted due to the convergence of Datacom and Telecom network applications [1]. A typical transceiver design includes both a transmitter and a receiver as shown in Fig. 1. The transmitter (TX) includes a PLL and multiplexer (MUX), which serializes the 16 bits parallel data if SF4 interface is used in the typical OC-192 applications. The synchronization clock is provided by a narrow bandwidth PLL. After serialization (or MUX), the data is sent to the photodiode through a laser driver (LD) as the interface to the single-mode Fiber or multi-mode Fiber for long distance data transmission. At the receiver side, the transimpedance amplifier (TIA) detects the photodiode current and converts it to voltage, and then the limiting amplifier (LA) amplifies and limits the voltage signal to a fixed level in order to increase the sensitivity of the clock data recovery (CDR) block. Finally, the recovered data is de-serialized into parallel data outputs for further framing or overhead processing.

Several 10G Bit/second (bps) transceiver IC have been recently reported [1]-[11]; many of them are fabricated in SiGe BiCMOS [1]-[5]. More recently, efforts have been reported to integrate the 10Gb/s CDR in CMOS technology for cost reduction and higher integration purposes [7]-[11]. However, these designs need a large off-chip integration capacitor to meet the jitter peaking and jitter tolerance defined in the Telecordia OC-192 standard. The off-chip capacitor increases the number of external components and pin count; also it couples noise from off-chip to the control voltage of the VCO in the CDR block. Another issue is that the bondwire inductor increases drastically the high-frequency impedance of the loop filter making the CDR more sensitive to HF noise.

As shown in [12], decreased area of on-chip capacitance can be realized by using active loop filters together with feedforward charge pumps. However, active loop filters increase the design complexity and jitter due to noise (mainly flicker) and offset contributions of active devices. In [13], a sample-reset loop filter is proposed to create the stabilization zero. The proportional path needs a narrow pulse to perform the reset function, but the narrow pulse generation is quite difficult in 10Gb/s CDR circuitry.

In this paper, a fully integrated CDR architecture that obviates the need of the large off-chip integration capacitor by adding two feed-forward paths to generate the stabilization zero is proposed. The required capacitor in this architecture is of the order of hundred picofarads (pFs), which is far smaller than that required by conventional loop filter configurations. Besides, resistive source degeneration techniques used in the auxiliary path reduce the effective input capacitance and alleviate the loading of the phase detector. RC source degeneration techniques are adopted for zero peaking and hence bandwidth extension in double edge D-Flip-flops (DEFF) of the phase detector (PD) designs is obtained. The CDR can recover the PRBS data with pattern length of $2^{15}-1$ and more than 0.5 unit interval peak to peak (UI$_{pp}$) total jitter (54.5ps eye closure by passing data through 9 inches FR4 PCB trace) and the total jitter of the recovered data is 22.7ps with a RMS jitter of 0.74ps.\footnote{For PRBS $2^{15}-1$ data, the eye closure is much heavier than 0.55UI and BER is difficult to be maintained as low as $10^{-12}$ unless an extra limiting amplifier is inserted between the FR4 PCB trace and the data input on-chip.}

The high frequency jitter tolerance of this design is over

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{fig1.png}
\caption{Optical transceiver block diagram.}
\end{figure}
0.31UI_{pp} by applying a PRBS data with a pattern length of 2^{31}-1. The CDR was fabricated in a standard 0.18μm CMOS technology. In section II existing solutions and the proposed architecture are compared. In section III, the building blocks are described in detail. The measurements results are discussed in section IV, and the conclusions are given in the last section.

II. DESCRIPTION OF THE ARCHITECTURE

A. Existing CDR architectures

In most OC-192 CDR ICs reported, PLL based CDR architecture is preferred over DLL based architecture because DLL is usually a first order system hence DLL based CDR has worse jitter tolerance and more jitter generation. When designing multiple channel receivers, it is advantageous to use the DLL [25], but this is not the scope of this paper. The CDR architecture can be divided into linear and binary [2]. Linear and binary CDRs use a Hogge Phase detector and Alexander phase detector, respectively. Typically, binary CDR is widely adopted in OC-192 receiver implementation for the following reasons: i) the D-flip-flop (DFF) in binary phase detector has inherently good match with the retiming DFF; ii) most linear phase detectors generate narrow pulses with widths proportional to the phase error between the timing alignment of the data and clock signals [5]. In a typical 0.18μm CMOS technology, the narrow pulses are difficult to generate and prone to process variations. The schematic of a typical linear CDR is shown in Fig. 2 [7], [9], [15].

![Fig. 2 Conventional PLL based CDR architecture](image)

The CDR includes two loops, a frequency acquisition loop (FAL) and a phase detection loop (PDL). The VCO’s frequency is tuned through two control mechanisms: proportional control which directly modulates the VCO control port by the phase detector (PD) output directly and integration control which slowly tracks (integrates) the variations at the output of phase detector through an integration capacitor. The proportional and integration controls have basically the same effect as using a charge pump together with a filter made of a series resistor and a capacitor [4]-[5].

B. CDR Architecture

The previously reported architectures need an off-chip loop filter or integration capacitor to meet the jitter specifications. The proposed CDR employs the conventional dual-loop architecture but the multiplexer is inserted before the charge pump CP1 and an auxiliary charge pump CPA is connected to the loop filter as shown in Fig. 3. During the revision process of this paper we learn that a similar technique has been reported in a patent recently filed [26].

![Fig. 3 Proposed CDR architecture](image)

The frequency acquisition loop uses a conventional linear phase frequency detector, while the phase detection loop adopts a half rate, double-edge DFF (DEFF) based binary phase detector which is similar to that reported in [6]. Although the DEFF phase detector may allow us to eliminate the frequency acquisition loop, the FAL was included to ensure enough frequency locking range, especially at the powering up stage. The switching between the FAL and PAL loops is controlled by a lock detector which works at the reference frequency of the FAL. Upon power-up, a successive-approximation register (SAR) type controller performs a coarse tuning for the VCO to within 1% frequency error of the target frequency by switching in or out a MIM capacitor bank and tuning a large coarse tuning varactor. Once the frequency difference between the internally divided clock and the reference clock is within 300ppm, the CDR will switch to the phase detection loop.

The phase detection loop uses a couple of charge pumps (CP1 and CPA). CP1 and loop filter enables the operation of a regular charge pump; the location of the zero-pole pair is determined by the time constants R(C1+C2) and RC2, respectively. In absence of the CPA, the spacing between the pole and zero frequency is entirely determined by the capacitive spread between C1 and C2. Low frequency noise signals injected into the loop filter are integrated by C1+C2 while high frequency signals are absorbed by C2 only. Therefore, it is desirable to increase as much as possible C2 to make the loop filter more robust against medium and high frequency noise current injected at node Vc in Fig. 3. Since C1 is often more than 15*C2 to ensure enough loop phase margin, often C1
values are in the range of nF, making very difficult to have full on-chip solutions. By adding the CPA more flexibility is introduced for the design of the loop filter and allows us to increase C2 for a given zero-pole location. As demonstrated in section III.C, another benefit is that the zero-pole location is still determined by C1/C2 but also by the ratio of the bias current used in CP1 and CPA, resulting in capacitance values that can be integrated into a single-chip. Also, high-frequency attenuation can be improved because C2 can be scaled up.

III. DESCRIPTION OF THE BUILDING BLOCKS

In this section, the design of the main building blocks of the proposed architecture is discussed.

A. Input Buffer & output buffer

Both the input and output buffer shown in Fig. 3 include five stages of CML amplifiers. Active inductor zero peaking is adopted every two buffer stages to avoid excessive equalization effect. To save chip area, active emulated inductors are employed [12]. Extensive simulations were done to ensure both enough bandwidth (> 7.5GHz) and small group delay variation (< 13ps). Lack of enough bandwidth, excessive equalization and large group delay reduces the eye opening and hence affect the signal integrity of the data.

B. Phase Detector Design considerations

The architecture is similar to that reported in [6], [18], as shown in Fig. 4. The double edged D flip-flop is constructed by using two current mode logic (CML) latches which are clocked with opposite clock phases, followed by a multiplexer that is selected by the input clock level of the CML latch. Zero peaking is a good solution to extend the bandwidth to tolerate higher input data rate such as 10Gb/s; in fact, series feedback has been successfully used in wideband Cherry-Hopper amplifier design [24],[26]. In this design, a multiplexer with RC source degeneration is used to extend its 3 dB bandwidth; the schematic is shown in Fig. 5. The effective small signal gain transfer function of the multiplexer is

$$Av(s) = \frac{G_mR_L}{1 + G_mR_s/2} \left( \frac{1 + sR_sC_s}{1 + \frac{sR_sC_s}{1 + G_mR_s/2}} \right)$$

(1)

Where $G_m$ is the transconductance of the input pair transistor; $R_s$ and $C_s$ are resistor and capacitor load, respectively. $R_s$ and $C_s$ are the degeneration resistor and capacitor, respectively, added to improve multiplexer performance. If the MUX is designed such that $R_sC_s \approx R_1C_L$, the zero cancels the output pole and the bandwidth increases without causing peaking in its frequency response. The RC source degeneration network decreases the input capacitance and thus eases the design of the preceding latch which sees smaller capacitance load. The expression for the multiplexer input capacitance yields

$$C_{in,\text{effective}} = \frac{C_{in}}{1 + G_mR_s/2} \left( \frac{1 + sR_sC_s}{1 + \frac{sR_s(C_s + C_{in})}{1 + G_mR_s/2}} \right)$$

(2)

where $C_{in}$ is the gate-source capacitance of the input transistors. The input capacitance is reduced by a factor $(1 + G_mR_s/2)$ at low and medium frequencies.

![Fig. 4. Half rate Phase detector (the Double edge DFF is shown in rectangle in dashed line) [6].](image)

![Fig. 5. Multiplexer with RC source degeneration used to extend its bandwidth.](image)

C. Charge Pump and loop filter

The typical charge pump topology is shown in Fig. 6a. The resultant transimpedance transfer function of the configuration, when taking the $I_C$ as the input and $V_{out}$ as the output, is found as

$$V_{out}(s) = \frac{1}{s(C_p + C_Z)} \left( \frac{1 + sR_ZC_Z}{1 + sR_ZC_pC_Z} \right) I_C(s)$$

(3)

and its main properties are given in table 1.
In this design, two feed-forward paths are added to generate the required zero and poles. A simplified schematic of the single-ended configuration is shown in Fig. 6b.

The charge pump on top of Fig. 6b generates the current $I_{cp}$ that is mainly integrated through the capacitor $C_2$; the bottom cell injects $I_{atp}$ current into the $R-C_1$ node to generate a voltage proportional to the phase detector output. The resultant filter’s output of the proposed configuration is found from the following expression

$$V_{ctl}(s) = \left[ \frac{1}{s(C_1 + C_2)} \right] \left[ \frac{1 + sRC_1(1 + \alpha)}{1 + sR\left(\frac{C_1C_2}{C_1 + C_2}\right)} \right] I_{cp}(s)$$

(4)

The location of the poles and zero are also given in Table 1. To compare both topologies two cases are considered. Unless otherwise specified, $I_c$ is the charge pump current of the typical loop filter with a single charge pump as shown in Fig. 5a.

i) Same low-frequency behavior ($C_p+C_2=C_1+C_2$ and $I_c=I_{cp}$). The conventional and proposed topology can be compared if its components are designed for the same loop transfer function; from Table 1 it can be found that these components are related as follows:

$$C_1 = C_Z - \alpha C_p \left( \frac{1 + (1 + \alpha) C_p}{\alpha C_Z} \right) \equiv C_Z - \alpha C_p$$

$$C_2 = \left[ 1 + \alpha \left( \frac{1 + \alpha C_p}{C_Z} \right) \right] C_p \equiv \left( 1 + \alpha \right) C_p$$

(5)

$$R = \frac{R_Z}{1 - \alpha C_p} \left[ 1 + \frac{(1 + \alpha) C_p}{\alpha C_Z} \right] \left( 1 + \alpha \right) \left( 1 - \frac{\alpha C_p}{C_Z} \right)$$

It is assumed in these expressions that $C_{2}>>C_{p}$ to ensure enough pole-zero spacing in the conventional charge pump. According to (5), reasonable values of $\alpha (1<<\alpha<<C_2/C_p)$ lead to $C_1<<C_2$ and $C_2>C_p$. Although to increase $\alpha$ is desirable because $C_1$ can be further reduced, its benefits are limited due to the large values required for $R$ when $\alpha$ approaches $C_2/C_p$. It can be shown that the smallest R is required when

$$\alpha = \frac{C_Z - 1}{C_p}$$

(6)

In this case, $R=R_Z/(1+C_2/C_p)$. The most remarkable benefit of this approach is the larger capacitance $C_1$ ($=1+\alpha C_p$) seen by the high-frequency noise current injected at the VCO’s control node $V_{ctl}$, making the circuit less sensitive to high frequency noise; e.g. $\alpha=9$ gives an additional 20 dB of attenuation for the high-frequency noise.

ii) Minimization of capacitors. The current used in the charge pump can also be scaled down and still be able to realize the required loop transfer function. If the bias current is scaled down, $I_c/I_{cp}=\beta>0$, then the low-frequency filter’s impedance, determined by $C_1+C_2$, can be scaled down by a factor $\beta$ as follows:

$$C_1 \equiv \frac{C_Z - \alpha C_p}{\beta}$$

$$C_2 \equiv \frac{(1 + \alpha) C_p}{\beta}$$

(7)

$$R \equiv \frac{\beta R_Z}{\left( 1 - \frac{\alpha C_p}{C_Z} \right)(1 + \alpha)}$$

It is clear that filter’s dominant capacitance $C_1$ can be further reduced due to the effect of CPA and the current scaling factor $\beta$. The downside is that the effective low-frequency filter’s impedance at the control node increases proportional to the...
current scaling factor. The low frequency impedance increase does not affect circuit’s performance if the bias current of the charge pump is scaled accordingly. Fortunately, the medium and high frequency impedance (determined by $C_z$) can be made even larger than $C_p$ if we select the scaling factors such that $1+\alpha\beta$. The main advantage of this approach is that the overall filter’s capacitance can be scaled down further while high frequency noise is filtered out by a larger capacitor. For a typical 10G CDR with conventional series resistor and capacitor filter, the integration capacitor $C_z$ is around 10-30nF even if the jitter transfer bandwidth is in the range of 4M-6MHz, which is very expensive to integrate on-chip. In the proposed implementation, the integration capacitor is around 100pF which is a realizable value in CMOS 0.18 $\mu$m technologies. The filter component values used for both topologies achieving the same filter output are given in table II. The silicon area saving of the proposed method is evident; the overall capacitance is reduced from 3 nF down to 140 pF.

**Table II. Component values for same charge pump-filter response.**

<table>
<thead>
<tr>
<th>Conventional Loop Filter</th>
<th>Proposed Loop Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_c=1.2$ mA</td>
<td>$\alpha=30$, $\beta=21$ $I_{cp}=60$ $\mu$A</td>
</tr>
<tr>
<td>$C_p=3$ nF</td>
<td>$C_z=100$ pF</td>
</tr>
<tr>
<td>$C_p=30$ pF</td>
<td>$C_z=40$ pF</td>
</tr>
<tr>
<td>$R_p=200$ $\Omega$</td>
<td>$R=190$ $\Omega$</td>
</tr>
</tbody>
</table>

In the real design, both charge pumps CP1 and CPA are differential architectures. The schematic of the charge pump CP1 is shown in Fig. 7(a); the common mode feedback system (CMFB), not shown in the schematic, fix the common-mode level of $V_o+$ and $V_o-$. The PMOS current sources are realized using a high swing cascode topology to increase the output resistance and reduce the current mismatches. This configuration achieves higher voltage swing (up to $1.1V_{pk-pk}$ in this design) than the classic cascode architecture.

The simplified schematic of the auxiliary charge pump is shown in Fig. 7(b). The resistor loads are balanced; the maximum differential voltage swing across each load resistor is given as $(4\alpha I_{cp})R$. Although there is no need for large input linear range (the binary PD only outputs either high or low digital state), the source degeneration resistors are added to reduce the effective input capacitance of the CPA such that the phase detector deals with smaller capacitive loading. Because the use of resistive terminations the need of a common mode feedback circuit is avoided.

The filter’s components are found according to the following considerations. Although the binary phase detector shows nonlinear characteristic, it can still be analyzed at the benefit of its highly overdamped PLL design to meet SONET jitter peaking requirements. The stability factor as defined in [5] and [15] should be far larger than 1 to ensure the loop stability. For the proposed architecture, the stability factor $\xi$ is defined as

$$\xi = \frac{2\alpha RC_p}{T_{bit}} \gg 1$$

(8)

Where $T_{bit}$ is the bit period. Because of the overload limited (Slew limited) characteristic of the nonlinear phase tracking loop, the effective bandwidth of the CDR loop follows the following relationship

$$BW = \frac{K_p I_{cp} R K VCO}{Jitter_{UI_{pk-pk}}}$$

(9)

where $Jitter_{UI_{pk-pk}}$ is the peak to peak jitter amplitude in an unit interval $(UI_{pk-pk})$ at the frequency of interest; $K_p$ is a fitting parameter that accounts for the delay of the phase detector, and $I_{cp}$ is the charge pump current.

The SONET jitter tolerance specification requires that the phase detection loop should have as large effective bandwidth BW as possible to tolerate high frequency jitter, while the in-band noise of the PLL finally limits the bandwidth because of the low pass characteristic of the PLL. A high current in the charge pump reduces the mismatch between the up and down current, while large bias currents result in more flicker and thermal noise. The charge pump current used in this design $I_{cp}$ is around 40$\mu$A, and the auxiliary cell uses a typical current of 500$\mu$A; $\alpha=12.5$.

**D. Quadrature LC VCO**

The core of the Quadrature LC VCO is similar to that reported in [16], [18]. As shown in Fig. 8, it is composed by 6
switch-able MIM capacitor banks for coarse frequency tuning, and a varactor for fine tuning. The varactor works in accumulation mode and is made of NMOS transistors fabricated into an N-well.

To satisfy the SONET jitter requirements, the maximum VCO phase noise must be computed. The relationship between phase noise ($\Delta f_n$) and VCO power spectrum $S_{\Delta f}(\Delta f)$ is derived in [25] by using the autocorrelation function of the timing jitter process and the Wiener-Khinchin algorithm. The RMS jitter of the VCO output signal is given as:

$$\sigma_J^2 = \frac{8}{\omega_0} \int_0^\infty S_\phi(t) \sin^2(\pi t) dt$$

and the power spectrum becomes $S_\phi(f) = 2 \ell(f)$. Since the phase noise follows a -20dB/decade shape around 1 MHz offset, it can be approximated as

$$\ell(f) = \frac{\epsilon_0}{(2\pi)^2}$$

Using the fact that

$$\int_0^\infty \sin^2(x) dx = \frac{\pi}{2}$$

It can be found that the RMS jitter is determined by $\sigma_J^2 = 2\epsilon_0\tau$; normalized by the VCO timing period yields $\sigma_J^2 = 2\epsilon_0/(2\pi f_0)^2$. Because the binary CDR is sensitive to the data transitions, $\tau$ can thus be approximated as the time span when consecutive runs of either “1” and “0” happen; the phase detector doesn’t update in this case (either high or low), thus the VCO jitter accumulates as free-running case.\(^2\) Assuming a maximum run length of 127 consecutive ‘1’s and ‘0’s data sequence, and making $\sigma_J < 0.01UI$ (Unit interval, 100ps for 10Gb/s bit rate), the phase noise of the VCO should be less than -90dBc @ 1MHz offset, which is similar to that derived in [22].

Due to process, voltage and temperature (PVT) variations the amplitude of the VCO output is not well controlled. To minimize this issue, an automatic amplitude control that uses a peak detector and a single-stage differential pair amplifier which adjusts the tail current of the LC tank maintains constant the VCO’s amplitude. The VCO’s output can also be externally adjusted through an array of programmable current sources.

The switching in-out of the MIM capacitor bank is controlled by a successive approximation register (SAR) block. Since the accumulation varactor is designed by putting NMOS transistor into a N-well, it can not be simulated directly as the inversion mode varactor which uses the transistor model. The varactor simulation is made easy by the model shown in Fig. 9. It uses a PMOS transistor which has the same size as the NMOS transistor in the varactor, and the $V_{BG}$ is the bandgap voltage source (around 1.2V); the bulk of the PMOS transistor is the tuning voltage input. The simulated varactor curve and the measured varactor curve are compared in Fig.10; deviations are less than 10% at 75°.

\(^2\) The charge pump can be tri-stated to alleviate the jitter accumulation, here we calculate for the worst case.
A Fully Integrated CMOS Clock Data Recovery IC for OC-192 Applications; J. Li, et.al.

\[ \text{pdf}_{RJ}(t, \sigma) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{t^2}{2\sigma^2}} \]  

(13)

While for DJ it can be written as

\[ \text{pdf}_{DJ}(t, W, \sigma) = 0.5 \left( \delta(t, -\frac{W}{2}) + \delta(t, \frac{W}{2}) \right) \]  

(14)

Where \( W \) is the magnitude of DJ, given as peak to peak. The TJ pdf can thus be derived as convolution of the DJ and RJ pdf as follows:

\[ \text{pdf}_{TJ} = \text{pdf}_{RJ} \otimes \text{pdf}_{DJ} \]  

(15)

By sweeping various sampling time \( t_s \), the BER can be estimated by calculating the cumulative density function as

\[ \text{BER}(t_s) = \int_{-\infty}^{t_s} \text{pdf}_{TJ}(t) dt + \int_{t_s}^{\infty} \text{pdf}_{TJ}(t) dt \]  

(16)

The BER bath-tub curve is displayed in Fig. 11. For robustness in the solution, it is desirable to have more than 0.5UI eye opening in the input data stream, such that the CDR can recover data with low BER. Fig. 11 shows that the eye opening is 0.45UI when the input data with a RJ of 0.008UI and a DJ of 0.44UI. For this case, the sampling instant falls into the inner region of the bath tub curve; the data can be recovered when the eye opening is over 0.44UI with a BER < 10^{-12}. For the combination of 0.02UI RJ and 0.6DJ, the eye opening is only 0.16UI for a BER < 10^{-12}, which is very tough even for the CDR to recover data with BER < 10^{-12}.

![Fig. 12 Chip microphotograph.](image)

The chip was fabricated in the TSMC 0.18\( \mu \)m, 1P6M CMOS process through the MOSIS educational service; Fig. 12 shows a micrograph of the CDR, which is pad-limited and occupies 2 x 2 mm² chip area with on-chip loop filter included. The entire characterization test is performed under room temperature. BER and jitter tolerance were performed by using an Anritsu MP1763C 12.5GHz pattern generator, Anritsu 1764C 12.5GHz error detector, and Agilent 71501C jitter analysis test systems.

The stressed data is generated by passing the data out of pattern generator to 9 inches FR4 PCB trace, such that DJ is added to cause eye closure.

Fig. 16 CDR jitter tolerance measurements with a peak to peak jitter of 8ps which is less than 0.008UI and conforms to the SONET jitter generation specification. Jitter tolerance is tested by passing the data pattern generated from the pattern
generator to the device under test (DUT), the recovered data is sent to BERT tester for BER test.

As shown in Fig. 16, for an input signal of 150mV_{pp} single-ended, a high frequency jitter tolerance greater than 0.3 UI_{pp} is achieved (at 80MHz of sinusoidal jitter frequency, the jitter tolerance is 0.31UI_{pp}), which confirms that, if there is over 0.5UI eye closure at the input data due to ISI distortion, the CDR can still recover data correctly. The CDR exceeds the SONET OC-192 jitter tolerance mask with over 100% margin for jitter frequency higher than 10MHz; for jitter frequency lower than 2MHz, the CDR exceeds the jitter tolerance test limit of the equipment used, where the data input is a 2^{31}-1 PRBS pattern.

The jitter transfer bandwidth (corner frequency) is 6.2MHz, and the jitter peaking is 0.07dB (less than 0.1dB defined in the SONET standard), thus it does not meet the SONET standard for the jitter transfer specification of 120KHz. However, as pointed out in [1] and [9], the jitter transfer characteristic can be shaped by a jitter attenuator PLL to shape the jitter transfer bandwidth of the clock recovered by the CDR. After the CDR locks to the input data at 9.953Gb/s rate, the phase detection loop can maintain lock even if the input data rate changes from 9.947Gb/s to 9.958Gb/s without going to frequency acquisition loop, which shows that the pull-out range of the phase detection loop is over 1100ppm. Fig. 17 shows the return loss of the input buffer, it is less than -13dB at 5GHz.

Including the buffers, the chip consumes 290mW with a 1.8V power supply. The chip is packaged in a 5 x 5 mm QFN package. Multiple pins are assigned to both power supply and ground to minimize the crosstalk effect. Performance of the chip is summarized in Table 2, which shows that this implementation consumes less power than previously reported solutions, except for the one reported in [6] which does not account the power consumption of the buffers. If the four on-chip inductors are replaced with two symmetric inductors, the chip area can be reduced even further. The jitter tolerance performance of the chip is approaching or even better than

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Table 2: Jitter Amplitude (UI_{pp}) vs. Jitter Frequency (Hz)

<table>
<thead>
<tr>
<th>Jitter Frequency (Hz)</th>
<th>OC-192 mask</th>
<th>Instrument limit</th>
<th>DUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>0.00 UI_{pp}</td>
<td>0.1 UI_{pp}</td>
<td>0.2 UI_{pp}</td>
</tr>
<tr>
<td>2 MHz</td>
<td>0.00 UI_{pp}</td>
<td>0.1 UI_{pp}</td>
<td>0.2 UI_{pp}</td>
</tr>
<tr>
<td>4 MHz</td>
<td>0.00 UI_{pp}</td>
<td>0.1 UI_{pp}</td>
<td>0.2 UI_{pp}</td>
</tr>
<tr>
<td>8 MHz</td>
<td>0.00 UI_{pp}</td>
<td>0.1 UI_{pp}</td>
<td>0.2 UI_{pp}</td>
</tr>
<tr>
<td>16 MHz</td>
<td>0.00 UI_{pp}</td>
<td>0.1 UI_{pp}</td>
<td>0.2 UI_{pp}</td>
</tr>
</tbody>
</table>

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In this implementation, the chip area can be reduced even further. The jitter tolerance performance of the chip is approaching or even better than
A Fully Integrated CMOS Clock Data Recovery IC for OC-192 Applications; J. Li, et.al.

V. CONCLUSION
A fully integrated 10-Gb/s CDR is implemented in a 0.18μm CMOS process. The design uses half rate architecture due to the relative low f0 (50GHz) of the CMOS process used. By using a new loop filter and charge pump configuration, the chip integrates all the components on-chip including the integration capacitor. Improved charge pump architecture with source degeneration, VCO with amplitude tuning and multiplexer scheme in double edged DFFs are the other techniques adopted to enhance the chip performance.

The CDR can recover data with a BER less than 10^-12 when the input eye closure is slightly above 0.5UIpp (Horizontal eye closure) and the recovered clock with peak to peak jitter less than 0.1UIpp. The CDR also exceeds the OC-192 jitter tolerance mask with high frequency jitter tolerance over 0.31UIpp. To the best of our knowledge, this reported implementation is the first fully integrated, PLL based 10Gb/s CDR in the literature.

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