Fast Placement for Large-scale Hierarchical FPGAs

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Abstract

In this paper, we propose a fast placer for FPGA placement on a new commercial hierarchical FPGA device. The novelty of this research lies in the application of a multilevel V-shape optimization flow including an architecture related cluster process and a constructive placement. The new placer can handle large-scale FPGA placement problem quickly. Experimental results show that the proposed placer can further reduced the wirelength average 28.3% compared with simulated annealing based tool while achieving near 5X speedup in runtime for the five largest MCNC benchmarks.

1. Introduction

Nowadays, increasing size and performance of FPGA makes implementation and deployment of more complex designs for dedicated applications. Large logic capacity used in modern FPGA makes development of efficient CAD tools a challenging feat. Placement and routing times of large FPGA can last many hours without any guarantee of successful completion. For FPGAs with million gates, the long compile times will delay the time-to-market obviously.

Some recent works concentrate on fast placement for FPGA. Callahan et al. [18] combine fast placement with module mapping for data path circuits by treating the problems jointly as a tree covering problem. Sankar and Rose presented an ultra-fast placement tool that aims to minimize area in [7]. Maidee et al. [17] proposed a fast partition-based placement algorithm, together with a post-refinement step based on a low-temperature simulated annealing. There have been other previous efforts trying to develop faster placement and routing algorithms [18, 2]. However, those existing fast FPGA placement tools can only treat medium-scale circuits and haven’t good quality-time trade-off of current large-scale circuits because of their simulated annealing schedule.

Our research is targeted at a recently commercial FPGA product [6]. We propose an architecture model of target FPGA device and try to address the problem of placing a circuit, which has been abstracted as a netlist on FPGA. In order to deal with the growing circuit logical scale, we contrive a quick and effective cluster-based two stage algorithm. This paper is organized as follows. In Section 2, we briefly describe target FPGA architecture and related definitions. In Section 3, we introduce the problem and outline our placement algorithm. Section 4 compares the run time and quality of our placement results to those of SA based tool. Finally we draw some conclusions and discuss future researches in Section 5.

2. Background

2.1. FPGA architecture Introduction

Different from ASIC design, FPGA design is always architecture-specific. The conventional FPGA mesh architecture has a symmetrical grid of logic blocks and routing channels on all four sides of the logic blocks. The hierarchical FPGA (H FPGA) architecture divides logic blocks and routing resources into different hierarchical levels. As shown in Figure 1: the lowest level of the hierarchy contains logic blocks and I/O pads while the routing resources contain switch blocks at different hierarchical levels. In a standard HFPGA architecture, each cluster at the \( i \)-th level consists of 4 subclusters at the level \( i-1 \). Each cluster at the level 0 represents an original logic block. Nowadays, HFPGAs are no longer just the favor of academics. A new FPGA product embedded with
H FPGA has been recently released by Agate Logic, a pioneering FPGA vendor.

2.2. Wirelength Evaluation Model

In our HFPGA architecture, each switch block or logic block is assigned with a quaternary code to indicate its position in the topology tree in Figure 2. The length of the code is decided by the total levels of the circuit and the current level of the switch block. As Figure 2 showed, the leaf nodes’ quaternary codes also represent physical positions of logic blocks in target FPGA device at the same time.

Traditional Manhattan distance based wirelength evaluation model is unfit for HFPGA architecture. We use a new level-discrepancy model to evaluate the wirelength.

The wirelength of all nets can be calculated by the following equations.

\[ D(B_i, B_j) = \sum_{l=1}^{N} d_l \beta_l \]  

\[ \text{WireLength} = \sum_{all}^{nets} C_{ij}^{net} [D(B_i, B_j)] \]

where \( D(B_i, B_j) \) is a single wire’s length between two connected logic blocks \( B_i \) and \( B_j \). \( d_l \) is 1 while the wire go through a switch block at level \( l \). \( \beta \) is normalized wirelength value [6] at each switch block’s level. \( C_{ij}^{net} \) presents traversing all wire in all net. Accumulating all \( D(B_i, B_j) \) of all nets, we can evaluate the total wirelength.

Table 1. Normalized wirelength at each level.

<table>
<thead>
<tr>
<th>level</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \beta )</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>10</td>
<td>20</td>
<td>34</td>
<td>60</td>
<td>114</td>
</tr>
</tbody>
</table>

3. Algorithm Description

In this section, we describe the placement algorithm and the specific factors that allow us to handle the large-scale placement problem quickly. We determine a set of strategies and their parameters which give us the best quality-time trade-off.

3.1. Multilevel Clustering Process

The first step of the placement algorithm is a bottom-up multilevel clustering process of logic blocks. The input to the clustering step is a netlist of \( N \) logic blocks and their interconnections, the number of clustering levels and the cluster granularities of each level. Initial netlist is coarsened by grouping logic blocks together to form a new netlist with fewer nodes and fewer interconnections. Each logic block or lower-level cluster belongs to a unique higher-level cluster.

The input netlist is represented by a hypergraph with each logic block being represented by a node and
each net represented by a hyperedge. A two-terminal net can transfer into two nodes and a weighted connected edge which weight is equal to 1. As to an r-terminal net \((r > 2)\), the edges of the net are usually weighted according to the size of the net \((r)\). Several weighting functions have been proposed, including \(2/r\), \(1/(r-1)\), or \(4/(r^2\text{-mod}(r,2))\) [13-15]. In essence, these weighting functions assign smaller weights to edges in larger nets. Our clustering algorithm uses the weighting function \(2/r\) for an r-terminal net.

The clustering algorithm has a greedy scheme. At each level, we set all blocks status to unclustered. Then we calculate each unclustered block pairs relationship. Next, we arrange those pairs relationship by descending order. The relationship value, \(v\) between each pair of unclustered blocks, is determined by two parts: (1) total number of connected edges between the pair, and (2) weighted values of those connected edges. The weighted function is mentioned above.

The maximal related pair of unclustered blocks are clustered to one block, their status also are updated to clustered. At the same time, all connected edges between the pair are eliminated and all edges starting from or aiming to this pair are updated. This process is repeated until all blocks’ statuses are set to clustered.

As mentioned above, we clustered two blocks into one block each time. We proceed in a similar manner to create further levels in the clustering hierarchy and receive different-scale results. Then we select clustering results of specific series of granularities as our next placement algorithm inputs. The cluster granularities selection is introduced followed.

Number of clustering levels \(L\), and cluster granularities at each level \(S_1, S_2, \ldots, S_L\) are determined by architecture parameters and circuit size. From the clustering results (netlists), we select \(L\) netlists of clusters and each cluster \(C_i\) has at most original \(S_i\) logic blocks from the initial netlist. We restrict the cluster granularities \((S_i)\) to be \((4, 16, 64, \ldots, 4^i, \ldots)\) in order to unify those values with standard HFPGA architecture parameters.

### 3.2. Placement Process

Given series of netlists of clusters and their interconnections, the constructive placement process determines positions for two kinds of clusters: (1) topological positions of high-level clusters (combined of lower level clusters or logic blocks), (2) physical positions of the lowest clusters (actual the logic blocks). The series of clusters could also be represented as a quadtree similar to the topological tree of FPGA device in Figure 2.

We also use quaternary coordinates for depicting each clusters’ topological positions and each logic blocks’ physical positions. The lower the cluster’s level is, the longer the cluster’s coordinate is. Firstly, the top-level clusters are arranged shortest codes at highest logic hierarchical level. Each sub-cluster’s code is composed of two parts: prefix inherited from its higher level clusters and progressively increasing suffix started with 0. The codes of the bottom-level clusters (logic blocks) are the longest in all clusters of the series of netlists. After the lowest level logic blocks have been arranged their coordinate, a placement result is achieved.

Figure 5. Coordinates Arrangement Result

Conventional fast algorithms always have a heuristic refinement process. This refinement is always based on simulated annealing. We have some tests on how this refinement works in our V-cycle placement framework. We record the placement results and run times of the largest five MCNC benchmarks with or without those above SA based refinement strategies. Some statistical data are illuminated as followed chart. Experimental results show that there is only average below 1% wirelength improvement while receiving an average compile-time penalty of over five times. So that we omit the SA-base refinement process in our algorithm for the best quality-time trade-off.

### 4. Result Analysis

To evaluate the algorithm’s performance, we place the largest five MCNC benchmark circuits. Table 2 demonstrates their characteristics. Meanwhile, we also implement a wirelength-driven simulated annealing algorithm placing those benchmarks for comparison. We adapt the annealing implementation in VPR [16]. In order to target on HFPGA, we replace its original...
cost function by the wirelength calculating formula (1b) in Section 2.2.

Under the same environment, we record the run times in Table 2. Columns Time represent the time consumptions on 3GHz Intel Xeon, Linux OS, 6GB memory. Columns Wirelength represent wirelength results of different algorithm. Column Ratio represents improvement ratios of our algorithm’s wirelength compared with SA’s.

From experimental results, we can see that our placer speeds up to near five times in runtime with average 28.3% improvement of wirelength compared with SA based tool.

Table 2. Results Comparison between Our Algorithm and SA

<table>
<thead>
<tr>
<th>Circuit</th>
<th># of logic blocks</th>
<th>SA implement</th>
<th>Our algorithm</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Time(s)</td>
<td>Wirelength</td>
<td>Time(s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ex1010</td>
<td>4598</td>
<td>333</td>
<td>630123</td>
<td>70</td>
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<tr>
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<td>344</td>
<td>586824</td>
<td>100</td>
</tr>
<tr>
<td>s38417</td>
<td>6406</td>
<td>581</td>
<td>642634</td>
<td>120</td>
</tr>
<tr>
<td>s38584.1</td>
<td>6447</td>
<td>629</td>
<td>785157</td>
<td>135</td>
</tr>
<tr>
<td>clma</td>
<td>8383</td>
<td>2085</td>
<td>948771</td>
<td>453</td>
</tr>
<tr>
<td>Avg. Improvement</td>
<td>4.46X</td>
<td>1</td>
<td>28.3%</td>
<td></td>
</tr>
</tbody>
</table>

5. Conclusions and Future Work

In this paper a V-cycle optimization flow and a clustering based constructive placement algorithm is presented to handle the placement problem for large-scale FPGA. Experimental results show that this algorithm can get superior wirelength results over the large circuits set of MCNC benchmarks compared with pure simulated-annealing based tool. Meanwhile, the presented algorithm has significant run-time speed up than simulated-annealing based tool.

In this work, the presented algorithm can only handle the placement problem efficiently for FPGA with homogeneous logic blocks and interconnection resources. However, industrial FPGA usually has heterogeneous cells such as RAM block, multipliers and complex IP cores, which will cause FPGA placement problem to be very difficult. In the future, the proposed algorithm can be extended to handle FPGA with heterogeneous architecture. More important, other critical rules, such as timing and power constraints can be added into the placement algorithm to further improve the large-scale FPGA placement.

References


