Is 3D Integration an Opportunity or Just a Hype?

Jin-Fu Li+ and Cheng-Wen Wu*

+National Central University/STC, Taiwan
*National Tsing-Hua University/STC, Taiwan
Outline

- Introduction
- 3D Integration Technology Using TSV
- Opportunities
- Challenges
- Conclusions
Introduction

- Integrating more and more transistors in a single chip to support more and more powerful functionality is a trend
  - Using 2D integration technology to implement such complex chips is more and more expensive and difficult

- Some alternative technologies attempting to cope with the bottlenecks of 2D integration technology have been proposed

- 3D integration technology using through silicon via (TSV) has been acknowledged as one of the future chip design technologies
3D Integration Technology Using TSV

- 3D integration technology using TSV
  - Multiple dies are stacked and TSV is used for the inter-die interconnection

- The fabrication flow of a 3D IC
  - Die/wafer preparation
  - Die/wafer assembly
# Die/Wafer Preparation

- **TSV technologies**
  - Via-first, via-middle, and via-last process flows
- **Comparison of process flow**

<table>
<thead>
<tr>
<th>Process Step</th>
<th>Via-First</th>
<th>Via-Middle</th>
<th>Via-Last</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV Drilling</td>
<td>Phase 1</td>
<td>Phase 1</td>
<td>Phase 3</td>
</tr>
<tr>
<td>TSV Insulation</td>
<td>Phase 1</td>
<td>Phase 1</td>
<td>Phase 3</td>
</tr>
<tr>
<td>TSV Metallization</td>
<td>Phase 1</td>
<td>Phase 2</td>
<td>Phase 3</td>
</tr>
<tr>
<td>FEOL Formation</td>
<td>Phase 2</td>
<td>Phase 2</td>
<td>Phase 1</td>
</tr>
<tr>
<td>BEOL Formation</td>
<td>Phase 2</td>
<td>Phase 2</td>
<td>Phase 1</td>
</tr>
<tr>
<td>Handler Attachment</td>
<td>Phase 3</td>
<td>Phase 3</td>
<td>Phase 2</td>
</tr>
<tr>
<td>Wafer Thinning</td>
<td>Phase 3</td>
<td>Phase 3</td>
<td>Phase 2</td>
</tr>
<tr>
<td>Backside Process</td>
<td>Phase 4</td>
<td>Phase 4</td>
<td>Phase 3</td>
</tr>
</tbody>
</table>
An Exemplary Via-Last Process

Source: V. F. Pavlidis and E. G. Friedman, “Three-dimensional integrated circuits”.

ASP-DAC-2010
Jin-Fu Li, EE, NCU
Electrical Characteristics of a TSV

- Capacitance of TSV

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>50</td>
<td>20</td>
<td>239.5</td>
</tr>
<tr>
<td>5</td>
<td>100</td>
<td>20</td>
<td>135.2</td>
</tr>
<tr>
<td>10</td>
<td>50</td>
<td>20</td>
<td>496.4</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
<td>20</td>
<td>288.3</td>
</tr>
</tbody>
</table>

Die/Wafer Assembly

- Bonding technologies for 3D ICs
  - Wafer-to-wafer (W2W), Die-to-Wafer (D2W), and Die-to-Die (D2D)
- Comparison of different bonding technologies

<table>
<thead>
<tr>
<th></th>
<th>D2D</th>
<th>D2W</th>
<th>W2W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yield</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Flexibility</td>
<td>High</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Production Throughput</td>
<td>Low</td>
<td>Good</td>
<td>High</td>
</tr>
</tbody>
</table>
Opportunities—Heterogeneous Integration

- Combine disparate technologies
  - DRAM, flash, RF, etc.
- Combine different technology nodes
  - For example: 65nm technology and 45nm technology

opportunities—high performance

- 3D integration technology can reduce the length of the long interconnections using TSV
- For example,

\[ L_{2D} = x + 2y \]
\[ L_{3D} = x + y + z \]
Opportunities—Low Power
3D IC allows much more IO resources than 2D IC

For example,

- Stacking of processor and memory

Bandwidth is limited by IOs

Many TSVs are allowed for high bandwidth transportation
Challenges—Thermal Management

- Heat removing of a 3D IC is much more difficult than that of a 2D IC
- Two key elements for thermal management
  - Thermal model
  - Design techniques
- Requirements of a thermal mode
  - High accuracy and low complexity
- Thermal design techniques
  - Thermal TSVs
  - Thermal wires
Challenges—*Yield Management*

- For W2W bonding technology, the yield of 3D ICs is the product of the yields of multiple die and the yield of stacking process.

\[
Y_{3D-W2W} = (Y_{2D})^n (Y_s)^{n-1}
\]

Challenges—Yield Management

- Effective approach for maximizing the yield of W2W integration is needed

Source: S. Reda, et al., IEEE TVLSI, 2009
Challenges—Testing

2D-IC Test Flow

1. Wafer Fab.
   - Wafer Test
   - Assembly & Packaging
   - Final Test

3D-IC Test Flow

1. Wafer Fab. 1
   - KGD Test 1
   - Stacking 1+2
   - KGS Test 1+2
   - Stacking (1+2)+3
   - KGS Test (1+2)+3
   - Assembly & Packaging
   - Final Test

2. Wafer Fab. 2
   - KGD Test 2
   - Stacking 1+2
   - KGS Test 1+2
   - Stacking (1+2)+3
   - KGS Test (1+2)+3
   - Assembly & Packaging
   - Final Test

3. Wafer Fab. n
   - KGD Test n
   - Stacking 1+2
   - KGS Test 1+2
   - Stacking (1+2)+3
   - KGS Test (1+2)+3
   - Assembly & Packaging
   - Final Test

Source: Dr. Erik Jan Marinissen

KGD: Known-Good Die Test
KGS: Known-Good Stack Test
Challenges—Testing

- **KGD**
  - Wafer-level KGD for 3D ICs is more difficult than existing KGD approaches for system-in-package (SiP)
  - The number of required test pads must be very small

- **KGS**
  - DFT methodology should be able to support the incremental test

- **Post-bond test (final test)**
  - Test optimization

- Furthermore, test optimization and integration for the overall test flow are also an important issue
Although many 3D process technologies have been proposed, some issues should be addressed before 3D technology is mature enough for high-volume manufacturing.

- Alignment accuracy
- Stacking process should not degrade the performance of the individual dies
- Wafer thinning
- High-quality and high density TSVs
- ...
Challenges——Infrastructure Issue

☐ CAD algorithms and tools for 3D IC designs should be developed
  - Efficient solutions that can support the complexity of 3D systems
  - Algorithms that include behavioral models for variety of components are needed
  - 3D IC design rules should be established
  - ....

☐ Standards
  - Various materials and processing technologies are involved in a 3D IC
  - Die or wafers can come from different IC manufacturers
Conclusions

- 3D integration technology using TSV is one of future design technologies
- It can offer many advantages over the 2D integration technology
- However, there are some challenges should be overcome before volume-production of TSV-based 3D IC becomes possible
- Also, some standards should be developed for 3D integration