Reliability investigation of AlGaN/GaN high electron mobility transistors under reverse-bias stress

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Impact of reverse-bias stress on the reliability of AlGaN/GaN high electron mobility transistors was investigated in this paper. We found that inverse piezoelectric effect could induce noisy characteristics of stress current, and the “critical voltage” increased with the drain–source bias in the step-stress experiments. Although the degradation of the gate leakage current and drain-to-source leakage current are non-recoverable, the maximum output current can recover almost completely through electron de-trapping procedure after stress. The de-trapping activation energy was estimated to be 0.30 eV by the dynamic conductance technique. The surface morphology of the electrically stressed devices was investigated after removing the gate metallization by chemical etching, and no pits or cracks under the gate contact were observed.

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1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are of tremendous interest for next generation high power and high frequency devices, mainly due to their high breakdown voltage [1] and high electron density [2]. One of the greatest impediments today preventing the further development of GaN HEMTs technology is its limited electrical reliability. In order to achieve solid reliability, a thorough understanding of the physical mechanisms behind device degradation is of great significance.

While degradation of GaN HEMTs has been studied extensively, the current understanding of the dominant degradation mechanisms is still limited. Joh and del Alamo [3] proposed that there is a critical drain-to-gate voltage beyond which GaN HEMTs begin to degrade in electrical-stress experiments. Transmission electron microscopy (TEM) imaging has revealed the formation of cracks and pits after OFF-state and ON-state stress of GaN HEMTs [4–6]. It has also been reported that electrical stress of GaN HEMTs results in the progressive appearance of electroluminescence (EL) spots on the gate edge [7–9]. Upon removal of the metallic contacts and the passivation layer, deep trenches were observed under the drain side edge of the gate by atomic force microscopy (AFM) [10]. Moreover, when the AFM and EL images are carefully overlaid, an almost perfect one-to-one corresponding between EL spots and pits on the surface is found [11], demonstrating that the appearance of EL spots in the AlGaN/GaN HEMTs during OFF-state stress is related to the progressive formation of pits on the surface of the semiconductor that woud act as leakage paths for gate current. Zanoni et al. [12] found that reverse-bias testing in GaN HEMTs at high negative gate voltage would induce a catastrophic increase in gate leakage current, but with only a slight degradation of drain current. Recent reports [13,14] suggested that for sufficient long stress time degradation occurs even below the “critical voltage”, and proposed that before permanent degradation gate current would become noisy. However, recovery property of device parameters beyond the “critical voltage” has been rarely investigated.

In this paper, step-stress experiments for $V_{ds} = 0$ V were performed firstly to study the degradation mode of the AlGaN/GaN high electron mobility transistors under reverse bias. Then the “critical voltage” dependence on the $V_{ds}$ and the impact of the step-stress on the breakdown characteristics of the device were investigated. The recovery properties of the leakage current and the maximum drain current were discussed subsequently. Finally, scanning electron microscopy (SEM) images of the material underneath the gate contact were analyzed.
2. Devices and experiments

The AlGaN/GaN HEMT epitaxial structure was grown by metal organic chemical vapor deposition (MOCVD) on (0001) sapphire substrate. The epitaxial growth was initiated with an AlN nuclear layer followed by a 1.3 μm unintentionally doped (UID) GaN layer. This was followed by a 1 nm thick AlN interlayer and a 29 nm thick Al0.3Ga0.7N barrier layer. The sample was capped with an in situ growth 1 nm thick GaN. The devices fabrication started with mesa isolation which was performed by reactive ion etching (RIE) with an etch-depth of 150 nm. Ohmic contacts consisting of Ti/Al/Ni/Au (22/140/55/45 nm) were annealed in a nitrogen ambient at 850 °C for 30 s, yielding a contact resistance typically around 0.5 Ω mm. Then surface passivation was done by depositing about 60 nm Si3N4 by plasma enhancement chemical vapor deposition (PECVD). Gate patterns were defined by optical lithography with Lg = 0.8 μm and Wg = 50 × 2 μm. The gate to source and gate to drain spacing are both 1.6 μm, forming a symmetric device structure.

Cross-section view of the device structure utilized in the step-stress experiments is given in Fig. 1. A typical device used in the study shows Ide of 900 mA/mm, Vth of −3.8 V and Gmmax of 225 mS/mm. In the step-stress experiments gate voltage Vg was stepped from −10 to −100 V at various drain voltage values while keeping source voltage Vs = 0 V. The stress currents Isource, Idrain and Igate were measured during each voltage step through the I/V-t sampling mode in Agilent B1500A semiconductor device analyzer. In the sampling measurements, source currents channels monitor current with a specified sampling interval. At the end of each step, some measurements were performed in a short time (less than 30 s) to characterize the device. Then the next voltage step was applied immediately.

3. Results and discussion

Fig. 2 shows the change in stress currents Idrain, Isource and Igate as a function of stress time in a step-stress experiment: Vg was stepped from −10 to −100 V in 5 V steps while keeping Vs = 0 V, the device was stressed for 5 min in each step. Insets: Zoom view of stress currents during the stress steps before and at the “critical voltage”.

Voltage (“Vg = −75 V”), stress currents increase sharply during each voltage step. The stress drain current Idrain and stress source current Isource show a sudden increase simultaneously above this “critical voltage” since the device under study in our experiment is symmetric in structure.

Fig. 3 shows the transfer characteristics of the device under study measured at the end of different voltage steps. The gate voltage Vg was swept from −6 to 2 V while keeping the drain voltage Vd = 10 V and source voltage Vs = 0 V during each measurement. It can be seen from Fig. 3(a) that, before the “critical voltage” is reached (see the curves measured after Vg = −10, −20, −30, −40, −50, −60, and −70 V), drain current on the OFF-state almost keeps constant. Then it increases sharply beyond the “critical voltage” (see the curves measured after Vg = −80, −90 and −100 V), mainly contributed by the leakage current from the channel to the gate diode. Besides, drain current on the ON-state decreases suddenly as the “critical voltage” is reached, as can be seen from the inset in Fig. 3(a). The maximum transconductance of the device under study also degrades apparently above the “critical voltage”, without any significant shift of the threshold voltage, as Fig. 3(b) shows.

Step-stress experiments for different values of Vds were also performed and the results are given in Fig. 4(a). It can be seen that, the critical drain-to-gate voltage Vds for the sudden degradation of gate leakage current depends strongly on the drain-to-source voltage. As Vds increases from 0 to 30 V, the critical voltage Vds increases from 76 to 94 V. To clarify these phenomena, electric field distribution in the AlGaN barrier layer at the critical voltages for different Vds conditions was simulated, as shown in the inset of Fig. 4(a). It is interesting to note that, the electric field at the drain side edge of the gate is almost the same (about 5 MV/cm), indicating that the degradation of the gate leakage current is induced by the high electric field around gate contact. Since the voltage applied to the gate electrode is more crucial to the device degradation than that applied to the drain side, the critical voltage for the Vds = 0 V state should be the lowest.

Drain-to-source breakdown characteristics of the fresh device and the devices after performing step-stress experiments are compared in Fig. 4(b). The breakdown voltage is defined as the drain-to-source voltage at which the drain current reaches 1 mA/mm with the gate biased at −10 V. It can be observed that the breakdown voltage decreases from 81 to 75 V when the device drives the Vds = 0 V step-stress, due to the increase of gate leakage current. The decrease in the breakdown voltage after performing
the step-stress for $V_{ds} = 30$ V is more prominent, which can be explained by the most severe degradation of the gate leakage current under this condition at the end of the step-stress experiments for various $V_{ds}$, as shown in Fig. 4(a).

Fig. 5 shows the degradation and recovery properties of the gate leakage current, drain-to-source leakage current and output current in a $V_{ds} = 0$ V step-stress experiment. Gate leakage current increases suddenly beyond the “critical voltage” (see the curves measured after $V_g = -80$, $-90$, and $-100$ V), which is indicative of the formation of a leakage path between the gate diode and channel. The drain-to-source leakage current also shows an obvious increase above the “critical voltage”, improving that the pinch-off property of the gate has degraded caused by the increase in gate leakage current. After two hours rest, almost no recovery can be observed in the gate leakage current and the recovery of the drain-to-source leakage current is also very slight, which means that the formation of the leakage path is permanent. The maximum output current $I_{d,max}$ also degraded suddenly beyond the “critical voltage”, and decreased by 30% at the end of the step-stress experiment. However, after two hours rest it almost recovered completely, to 98% of its original value.

Based on the results presented above, we propose the following model to explain the degradation mode of the device under step-stress. When the gate diode is reversely biased, traps may be randomly generated within AlGaN layer due to the high electric field under the edge of the gate. The electrons that tunnel from the gate electrode can inject into these traps at the very beginning of each voltage step as shown in Fig. 6(a), resulting in the increase of stress gate current. But once the traps are all filled with negative charges, gate current will decrease immediately, which explains the recoverable decrease of the stress gate current during each voltage step in Fig. 2. Beyond the “critical voltage”, crystallographic defects can be formed in the AlGaN barrier due to the inverse piezoelectric effect [3]. When the defects in the AlGaN barrier become excessive, they would overlap with each other and result in the noisy characteristics of stress gate current in Fig. 2. As the experiment proceeds, a leakage path may be induced between the gate diode and the channel, contributing to the sudden increase of stress gate current and the OFF-state drain current as shown in Figs. 2 and 3(a) respectively.

Under high reverse bias, a large amount of electrons tunnel from the gate electrode would inject into the traps induced by the inverse piezoelectric effect in the barrier beyond the “critical voltage”. Electrons that captured by the traps would deplete the sheet carrier in 2DEG through modifying the electrostatics of the channel, very similar to the “virtual gate” process [15].
decrease in the sheet carrier density on the channel results in the increase of drain and source access resistance and leads to the sharp reduction of the ON-state output current and the maximum transconductance in Fig. 3. After the stress is removed, the trapped electrons can be thermally activated during the room temperature storage and de-trapped from the AlGaN barrier, as shown in Fig. 6(b). Similar recovery characteristics of the output current at room temperature have also been observed by other authors [16]. Besides, the de-trapping process can be accelerated by shining microscope light and UV light, or heating the device.

In our previous work [17] we have proposed that traps under the gate contact can be characterized by measuring the frequency dependent capacitance and conductance with the gate biased at the accumulation region, and the well-established method is directly applied in this paper to obtain the de-trapping activation energy. Since the normal structure devices are very hard to perform the C–V measurements due to the small area of the gate contact, FAT–FETs on the same wafer were used instead. The fabrication process and device structure of the FAT–FETs are all the same as the above mentioned normal structure devices, except that their gate length are 50 μm. Step-stress experiments for $V_{ds} = 0$ V were performed firstly until the sudden degradation of gate leakage current occurred to induce traps in the barrier layer. Then the frequency dependent capacitance and conductance measurements

Fig. 5. Degradation and recovery properties of the gate leakage current (a), drain-to-source leakage current (b) and output current (c) in a $V_{ds} = 0$ V step-stress experiment. Curves measured before stress, after $V_g = -80$ V, $V_g = -90$ V, $V_g = -100$ V, and after two hours rest of the stress are compared.

Fig. 6. Energy band diagrams illustrating the electron trapping under reverse bias (a) and de-trapping when the stress voltage is removed (b).
were conducted at the accumulation region ($V_g = 0$ V). The parallel conductance $G_p(\omega)$ is related to the measured capacitance $C_m$ and conductance $G_m$ through the following relation:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_b^2}{G_m^2 + \omega^2 (C_b - C_m)^2}$$  \hspace{1cm} (1)

where $\omega$ is the radial frequency and $C_b = 54 \text{ pF}$ representing the static-state capacitance of the device. Assuming a single energy level, trap time constant $\tau_T$ of 0.59 $\mu$s and trap density $D_T$ of $5.55 \times 10^{15} \text{ cm}^{-2} \text{ eV}^{-1}$ were derived with the fitting equation given in Fig. 7. The trap state activation energy $E_T$ was derived from the expression:

$$\tau_T = (\sigma_T N_c m_T)^{-1} \exp \left( \frac{E_T}{kT} \right)$$  \hspace{1cm} (2)

In which capture cross section of trap states $\sigma_T = 3.4 \times 10^{-15} \text{ cm}^2$, the density of states on the conduction band $N_c = 4.3 \times 10^{14} \times T^{3/2} \text{ cm}^{-3}$, and the average thermal velocity of the carriers $v_T = 2.6 \times 10^6 \text{ cm/s}$ were used [18]. De-trapping activation energy of about 0.30 eV below the conduction band at room temperature was derived subsequently. Since the traps are mostly fast traps with time constant about 0.59 $\mu$s, the nearly total recovery of the maximum output current in about two hours can be easily understood.

Finally, the surface morphology of electrically stressed devices was investigated by removing the passivation and gate metallization by chemical etching. The etching procedure was the same as indicated in Ref. [19]: HF:H$_2$O (1:10) for the removal of SiN, aqua regia solution (HCl:HNO$_3$ 3:1) for the removal of the metals, and piranha solution (H$_2$SO$_4$:H$_2$O$_2$) for a final cleansing of the chip surface. The regions of the semiconductor surface where source and drain contacts used to be before their removal are easily identifiable in the scanning electron microscopy (SEM) image (see Fig. 8). However, SEM canning of the material underneath and around the gate fingers of many devices reveals no presence of pits or cracks, which is quite opposite to reports of Refs. [11,19]. In fact, neither pits nor cracks were found at the drain-side gate edge of the high-voltage stressed devices in Refs. [20,21]. It is assumed that although a large amount of defects generated in the AlGaN barrier due to the inverse piezoelectric effect above the "critical voltage", physical damage to the semiconductor was still not induced in our experiments. The appearance of vast defects increases the gate leakage current by forming leakage path and reduces the maximum drain current by trapping electrons. However, the degraded maximum output current is able to recover almost completely through the electron de-trapping procedure since the transport property of the channel was not damaged.

4. Conclusion

In conclusion, we found that inverse piezoelectric effect can induce the noisy characteristic and sharp increase of the gate leakage current around the "critical voltage". Although the sudden degradation of the gate leakage current occurred at different "critical voltages" in the step-stress experiments for various $V_{ds}$ values, the electric field at the drain-side edge of the gate is almost constant. Beyond the "critical voltage" a leakage path may be induced in the barrier layer, contributing to the permanent degradation of schottky leakage current and drain-to-source leakage current. The maximum drain current also degraded apparently caused by the electron trapping under high reverse-bias, but could recover almost totally after stress through the de-trapping procedure. The de-trapping activation energy was estimated to be 0.30 eV by the dynamic conductance technique. SEM canning of the material underneath and around the gate fingers after metal removal reveals no physical damage.

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