The Failure Mechanism of High Voltage Tolerance IO Buffer under ESD

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ABSTRACT

In this paper, the real-time IV measurement and TCAD simulation were used to study why the ESD performance of the HVT IO circuit is different from the ST NMOS device. The real-time IV measurement shows that top gate induced voltage of the ST NMOS in HVT IO circuit under ESD zapping event is much higher than the ST NMOS device. The simulation shows that high gate voltage will induce the current crowded in the channel region, so as to degrade the device ESD performance. This phenomenon is called as "gate voltage-induced current crowding" (CVICC) effect. However, it is also found with non-silicide SID structure and increasing the RPO dimension at the drain region of top NMOSFET can effectively reduce the CVICC effect and push the currents to flow through bulk parasitic bipolar transistor. As a result, ESD failure threshold can be much improved.

INTRODUCTION

The stacked NMOSFET (ST NMOS) was firstly proposed by S. Voldman [1] for tolerating a high voltage across the output driver in mixed-voltage IO circuits. It has been reported that high voltage tolerance (HVT) IO buffer (Fig. 1a) is more vulnerable to ESD damage than the regular IO buffer (Fig. 1b) for positive ESD/Vss zapping event [2-4]. The authors considered that stacked NMOSFET structure would lead to higher \( V_{	ext{th}} \) and \( V_{	ext{max}} \), and then resulted in worse ESD failure threshold than that of the single NMOSFET structure [2], [4]. However, by comparing the high current I-V characteristics (Fig. 3) of the ST NMOS devices (Fig. 2a) and the grounded gate NMOSFET (GGNMOS in Fig. 2b), the curves will match to each other at the high stress current level (22A) if the devices have the same silicide-block (RPO) width. It is also found that \( I_{	ext{t}} \) of GGGNOMOS is only a little higher than that of the ST NMOS device if the two devices have the same RPO width. Because there is no current flowing from floating-well PMOSFET to Vss (Fig. 1a), the HVT IO circuit during +ESD/Vss zapping event still makes use of the ST NMOS device to discharge ESD current. Therefore, the real failure mechanism of HVT IO circuit can not be well explained by the argument, that is the ST NMOS device has the higher \( V_{	ext{th}} \) and snapback voltage (\( V_{	ext{op}} \)) [4].

To study the failure mechanism of the HV IO, the high current IV characteristics of the HVT IO circuit (Fig. 1a) and the ST NMOS device (Fig. 2a) are compared. Although the discharge elements of the two test structures are the same (ST NMOS), we find that ESD discharge behavior of the HVT IO circuit is much different from ST NMOS device. By comparing the schematics in Fig. 1a and Fig. 2a, the primary difference between HVT IO circuit and ST NMOS device is the top gate's configuration. For HVT IO circuit, the top gate of the ST NMOS is connected to Vcc. For ST NMOS device, the top gate is floating. It is then suspected that the gate potential during ESD transient should be much different, and then lead to different ESD failure threshold.

To study the influence of gate potential on the device ESD performance, the real-time voltage waveforms of the HVT IO circuit and ST NMOS device under TLP stress were measured. Based on the measured gate voltages, the 2-D simulators (SUPREM-4 and MEDICI) were used to study the influence of the gate potential on the current distribution of the ST NMOS device under ESD zapping event to gain insight of the HVT IO circuit failure mechanism.
Fig. 3 High current I-V characteristics of GGNMOS and the ST NMOS device in Fig. 2. (The layout of the structure is shown in Fig. 5.)

EXPERIMENTS

The \( V_{th} \), \( V_{w} \) and \( I_{s} \) measurements are performed on the Barth Transmission-line pulse (TLP) system. System components include the control box/pulse generator, digitizing oscilloscope, pico-ammeter, and high voltage power supply. A 100nsec current pulse was applied to the device and the stress current level was increased continuously until the device failed. The failure criterion was defined as the drain junction leakage current \( \geq 1 \mu A \) at \( 3.3 \) V.

The HBM and MM tests were performed on Key-Tek ESD tester. The tester applied a series of 3 \( \times \) ESD/\( V_{ss} \) pulses to the tested device and increased the stress voltage level continuously until the device failed. The failure criterion is defined as the drain junction leakage current \( \geq 1 \mu A \) at \( 3.3 \) V.

To gain more detailed insight into the complex interaction between ESD and the device, the apparatus as shown in Fig. 4 was used to simultaneously measure the voltage and current waveforms of the ST NMOS device and HVT IO circuit under different TLP stress events. The stress current and drain voltage waveforms were measured and recorded by the oscilloscope of the TLP system, and the gate voltage waveform was measured and recorded by another oscilloscope (Tektronix TEK 664A). The layouts of these test devices used in this work are the multi-finger ladder structures. The devices were fabricated with dual gate oxide and CoSi2 silicide modules. The tested devices were covered by resist protection oxide (RPO) to produce the ballast resistors for enhancing the device ESD performance. Because the ESD performance is RPO layout dependent, two kinds of RPO layouts were designed to study the influence of the RPO layout on ESD sensitivity. For structure I (Fig. 5(a)), the non-silicide region locates from the drain to source of the top NMOS. For structure II (Fig. 5(b)), the non-silicide region only locates at the drain side of the top NMOS.

RESULTS

a. High Current IV Characteristics and ESD Performance Comparison

To explore the mechanism difference between the HVT IO circuit and the ST NMOS device under ESD zapping event, the high current IV characteristics of the HVT IO circuits (Fig. 3).
1a) and the ST NMOS devices (Fig. 2a) are compared. Fig. 6-8 show the high current IV characteristics of the ST NMOS devices and HVT IO circuits with different RPO layout structures. Based on the IV curves, $V_{th}$, $V_{pp}$ and $I_{Q}$ of these tested devices can be extracted and shown in Table-I. In addition to the RPO layout splits and ESD performances are also summarized in Table-I.

Although the discharge elements of the HVT IO circuit and ST NMOS device are the same (ST NMOS), the high current IV characteristics and ESD performance of the HVT IO circuit are very different from those of the ST NMOS device. From Table-I, Fig. 6, Fig. 7 and Fig. 8, some interesting phenomena can be found:

1. For a given stress current and a given RPO layout split (Fig. 6-Fig. 8), the operation voltage after the $V_{th}$ of the HVT IO circuit is higher than the ST NMOS device.
2. The ST NMOS devices are always with larger $V_{pp}$, higher $I_{Q}$ and better HBM or MM failure threshold but lower $V_{pp}$ than those of the HVT IO circuits.
3. For structure I, the increasing in the RPO width can much improve the ESD failure threshold of the HVT IO circuits to acceptable values (HBM > 4KV and MM > 200V). On the contrary, the ST NMOS devices are not sensitive to the RPO width and layout.
4. For a given RPO width (2um in Table-I), the ESD failure threshold of the HVT IO circuit with structure II is only half of the HVT IO circuit with structure I.

### Table-I

<table>
<thead>
<tr>
<th>Fig.</th>
<th>Stru.</th>
<th>RPO</th>
<th>$V_{th}$</th>
<th>$V_{pp}$</th>
<th>$I_{Q}$</th>
<th>HBM</th>
<th>MM</th>
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<tr>
<td>HVT</td>
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<td>1um</td>
<td>7.57V</td>
<td>7.06V</td>
<td>0.25A</td>
<td>&lt;5KV</td>
<td>&lt;50V</td>
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<tr>
<td>ST N</td>
<td>2a</td>
<td>1um</td>
<td>8.64V</td>
<td>5.43V</td>
<td>2.75A</td>
<td>5.5KV</td>
<td>250V</td>
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<tr>
<td>HVT</td>
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<td>2um</td>
<td>8.14V</td>
<td>5.9V</td>
<td>2.46A</td>
<td>5KV</td>
<td>250V</td>
</tr>
<tr>
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<td>5.38V</td>
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<td>300V</td>
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<td>7.55V</td>
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<td>1.38A</td>
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<td>5.6V</td>
<td>2.92A</td>
<td>5.5KV</td>
<td>250V</td>
</tr>
</tbody>
</table>

### Fig. 6

High current IV characteristics of the ST NMOS device and HVT IO circuit with structure I (RPO 1um) in Fig. 5.

### Fig. 7

High current IV characteristics of the ST NMOS device and HVT IO circuit with structure I (RPO 2um) in Fig. 5.

### Fig. 8

High current IV characteristics of the ST NMOS device and HVT IO circuit with structure II (RPO 2um) in Fig. 5.

### b. Real-Time IV Characteristics

From Fig. 1a, Fig. 2a and the results in above section, we known that the only difference between the HVT IO circuit and ST NMOS device under ESD zapping is the gate configuration. For HVT IO circuit, the top gate is connected to Vcc. For ST NMOS device, the top gate is floating. But, why the gate configuration will result in such different discharge behaviors between HVT IO circuit and ST NMOS device is still unknown. To explore what difference between HVT IO circuit and ST NMOS during TLP stress, the real-time voltage waveforms of the top NMOS's drain and gate terminals of the ST NMOS device and HVT IO circuit under TLP stresses are recorded and shown in Fig. 9 and Fig. 10. In this measurements, the used structure for HVT IO circuit and the ST NMOS device is the structure I with 2um RPO width. The stress current levels are 200mA, 500mA and 1A, respectively.

For a given current level, the drain voltage of the HVT IO circuit (Fig. 10a) is only a little higher than that of ST NMOS device (Fig. 9a). But, the gate voltage waveforms of the HVT IO circuit are apparently different from the ST NMOS device (Fig. 9b and Fig. 10b). For the ST NMOS device, the induced gate voltages are all below 1.7V within the snapback region (from 40ns to 120ns), and decay to 0 volt immediately after the end of the TLP pulse. For HVT IO circuit, however, the gate voltages within snapback region are
higher than 8V, and the pulse duration time of the gate voltage (>150nsce) is longer than the TLP duration time (100nsec).

MECHANISM

To explain the observed behaviors of the HVT IO circuit under TLP stress in above sections, a schematically physical model is proposed as shown in Fig. 11.

Fig. 11 The schematic of HVT IO circuit under TLP.

a. HVT IO Circuit Device

Figure 11 shows that the floating N-Well PMOS (P1) of HVT IO circuit has two parasitic diodes. One diode is drain-to-N-Well diode (D_{DNW}) and the other diode is source-to-N-Well diode (D_{DSW}). In addition, there also exists a parasitic capacitor (C_c) between Vcc and ground. Before the device into the snapback region (time <50nsec in Fig. 10a), the current flows through the channel of the P1 to charge up the parasitic capacitor C_c, and then raise the voltages of Vcc pad and top gate simultaneously, as shown in Fig. 10b. Finally, the HVT IO circuit transistor goes into the snapback region and clamps the TLP pulse to a low voltage after the time 50nsec in Fig. 10a since the parasitic npn bipolar transistors of the ST NMOS had been turned on. After this transient point, the Vcc voltage became higher than the drain voltage. The channel of the P1 turned off and the drain to floating N-Well diode D_{DNW} was based at reverse mode. Thus, the current paths of the capacitor C_c are blocked. Without the discharge current path, the gate terminal would be sustained at high voltage until the leakage current of the HVT IO circuit transistor discharged all of the stored charges in the capacitor C_c. Thus, the duration times of the observed gate voltages are all longer than the TLP duration time (100nsec).

b. ST NMOS Device

Fig. 9a shows that three TLP pulses are all clamped at constants by the ST NMOS device and the top gate voltages are also kept at constants (Fig. 9b) after the device gone into the snapback region. This phenomenon, that is TLP will induce a large constant voltage (≈7.8V in Fig. 7) to the gate of the top NMOS as the ST NMOS device is operated at the snapback region, can not be simply explained by the capacitor coupling effect. In fact, the induced gate voltage of the top
NMOS is very small if the applied voltage is below the $V_T$ of the ST NMOS device. Fig. 12a shows the real-time IV of the ST NMOS device under TLP stress event for the condition that applied voltage is smaller than the $V_T$ of the ST NMOS device. The induced gate voltage of the top NMOS is only -0.05V (Fig. 12b).

Figure 13 shows the equivalent circuit of the ST NMOS device under TLP stress event. If the applied voltage of the TLP is higher than the $V_T$ of the ST NMOS device, the voltage couples through the capacitors to raise up the gate voltage of the top NMOS (1.5V within the time 30nsec to 40nsec in Fig. 9b). Because the induced gate voltage is higher than the threshold voltage of the top NMOS, the channel of the top NMOS would be turned on to give rise of the drain voltage of the bottom NMOS (Mid-N+ in Fig. 13). And, this argument can be verified by the TCAD simulation result. Fig. 14a shows the simulated IV of the ST NMOS device under the current stress for the top gate voltage 1.5V. Corresponding to each IV point in Fig. 14a, the simulated voltage of the Mid-N+ is shown in Fig. 14b. As the ST NMOS device is operated at the snapback region, the parasitic npn bipolar transistor of the Bottom NMOS also can be turned on. As shown in Fig. 15b in the following section, it can be observed that some of the currents can flow from the drain of the top NMOS through the Mid-N+ to the source of the Bottom NMOS to result in a voltage drop across the Mid-N+ (Fig. 14b). Thus, the gate voltage of the top NMOS can not be pulled down and kept a constant.

![Fig. 13 The equivalent circuit of the ST NMOS device under TLP.](image)

![Fig. 14 a. The simulated IV of the ST NMOS device under TLP, b. the simulated voltage of Mid-N+ in Fig. 13.](image)

Fig. 12 (a) The real-time I-V of the ST NMOS device under TLP if the applied voltage < $V_T$ of the ST NMOS. (b) The coupled voltage of the top gate.

**c. Gate Voltage-Induced Current Crowding (GVICC) Effect**

From Fig. 1a and above discussions, it can be understood that the primary ESD protection device for +ESD/Vas zapping of the HVT IO circuit is the ST NMOS since the current cannot flow through the floating Well PMOS to Vss. The only difference between HVT IO circuit and ST NMOS devices during ESD zapping event is the top gate voltage of the ST NMOS. Thus, it allows us to use the ST NMOS to simulate the current distribution of the HVT IO circuit during ESD zapping event.

Based on the measured gate voltages in Fig. 9b and...
the current does not only flow through the channel region but also through NMOS devices with larger heat generation at this localized region will easily result in high heat generation of the ST NMOS device at low gate bias. That is why ST NMOS devices have better ESD failure threshold than that of HVT IO circuit transistor, due to this GVICC effect.

For the case with high gate bias (Fig. 15a), most currents will flow through the channel region, not through the parasitic npn bipolar transistors of the top NMOS. This high channel current can generate a lot of electron-hole pairs due to high impact ionization. More holes can flow into the substrate, so as to reduce device trigger voltage $V_{TH}$. However, due to most of the current including diffusion and drift currents are confined in the channel region near the surface. This decreases the effective region for discharging current to result in high stress current density. Thus, it will cause larger $V_{TH}$ and smaller $I_{ch}$ as the top gate of the ST NMOS has high gate voltage. Moreover, due to very limited Si volume at the channel region, high heat generation at this localized region will easily result in lower ESD failure threshold. So, the GVICC effect can explain why the HVT IO circuit failed at lower voltage ESD zapping event very well.

However, for the case with low gate bias (Fig. 15b), the current does not only flow through the channel region but also can flow through the npn bipolar transistors of the top NMOS (npn-1 and npn-2 in Fig. 16). Smaller gate voltage will also induce less electron-hole pairs, so as to more difficult to trigger on the parasitic npn bipolar transistor. Thus, the ST NMOS devices are always with larger $V_{TH}$ than the HVT IO circuit (Table I). Moreover, because the ESD current can flow along the N+ drain junction of the top NMOS uniformly, the effective region for discharging current is apparently increased, so as to reduce the stress current density significantly. Thus, it will cause smaller $V_{TH}$ and larger $I_{ch}$ as the top gate of the ST NMOS has low gate voltage. Comparing Fig. 15a with Fig. 15b, we can observed that current distribution of the ST NMOS device at low gate bias is much uniform than the ST NMOS device at high gate bias. Thus, the heat generation of the ST NMOS device at high gate bias should be much higher than that of ST NMOS device at low gate bias. That is why ST NMOS has better ESD failure threshold than that of HVT IO circuit transistor, due to this GVICC effect.

d. ESD performance vs. RPO Layout Structure

The effect of RPO dimension (Fig. 5a) on ESD failure threshold can be explained as following. Increasing the RPO width will increase the series drain resistor (ballast resistor) so as to increase the $V_{TH}$ and $V_{PP}$. However, most of the ESD currents will also be pushed to flow through the N+ drain to PW (N+/PW) junction by this ballast resistor, and discharged by the parasitic npn bipolar transistors. Therefore, the ESD failure threshold can be improved due to high Si volume-induced lower heat generation. Therefore, the ESD performance of HVT IO circuit with 2um RPO width can be observed to be apparently higher than that of HVT IO circuit with 1um RPO width (Table-I).
When the source region of top NMOS is with silicide (Fig. 5b), the resistance of ballast resistor will be decreased. Without high resistance of ballast resistor, a lot of the ESD current will flow through the turned-on NMOS N1 to npn-3 bipolar transistor if the top gate of ST NMOS device is biased at high voltage. Because the collector region of npn-3 bipolar transistor is very small, most of the ESD current was confined in the small volume. It will result in the increase of stress current density and worsen the device ESD performance significantly. That is why the high current I-V characteristic of the HVT IO circuit is apparently different from that of ST NMOS device (Fig. 8).

If there is no silicide formation at source region as shown in Fig. 5a, only part of the currents can flow through the turned-on NMOS N1 to npn-3 bipolar transistor even a high voltage is applied to the top gate of ST NMOS device. But most of currents will flow through the npn-2 bipolar transistor since the ballast resistor should lead the current to flow through the turned-on NMOS N1. Unlike the high current I-V curves in Fig. 6 and Fig. 8, Fig. 7 shows that high current I-V characteristic of the HVT IO circuit is very close to that of ST NMOS device. As a result, the top NMOS without silicide formation at source/drain (S/D) regions will have better ESD failure threshold, especially for the case with HVT IO circuit.

e. Failure Analysis

To verify above model, physical failure analysis (FA) is performed to the ESD transistors, and the results are shown in Fig. 17 and 18. Top-view SEM photograph shows that filament formation starts from the drain and ends at the source of the top NMOS. It implies that most of the ESD current flowed through the turned-on NMOS N1 but only a little ESD currents can be discharged by the npn bipolar transistors (npn-1 and npn-2). The cross-section SEM photograph shows that damaged sites (marked by arrows) only locate at the S/D junctions of the top NMOS. It proves that a lot of currents have passed through the channel region near the surface of the top NMOS N1 to raise the junction temperature and generate the defects in these S/D regions [5].

CONCLUSIONS

Although the primary ESD protection device for +ESD/−Vss zapping of the high voltage tolerance (HVT) IO buffer is the stacked nMOSFET (ST NMOS), we found that ESD performance of the ST NMOS device is much robust than the HVT IO circuit. From the comparisons of the real-time IV measurements and TCAD simulation, why the ESD discharging behavior of the HVT IO circuit is different from the ST NMOS device and the failure mechanism of the HVT IO circuit under ESD had been explored. For HVT IO circuit, the top gate is connected to Vcc. And during ESD zapping event, we found that Vcc pad would be pulled-up to high voltage (>8V). As a result, the channel of the top nMOSFET would be turned-on to result in the current crowding in the channel region, but discharges the little current through the parasitic npn bipolar transistor in the snapback region. This phenomenon is called the "gate voltage-induced current crowding" (GVICC) effect. It leads to lower trigger voltage (Vt) but higher snapback voltage (Vs) and worse ESD failure threshold. For the ST NMOS device, only small ESD-induced gate voltage (0.7−1.5V) can be observed. Therefore, most of the ESD currents flow through the npn bipolar transistors. It results in higher Vt and lower Vs, but better ESD failure threshold.
REFERENCES


