A New Pre-Driver Design for Improving the ESD Performance of the High Voltage Tolerant I/O

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ABSTRACT

The gate voltage-induced current crowding (GVICC) effect [1] had been found as the root cause of that high voltage tolerant I/O (HVT I/O) failed at low-voltage ESD event. Based on this finding, a new pre-driver design is proposed to pull down the voltages of top gate and bottom gate of the cascode NMOS to 0V during ESD zapping event for eliminating the GVICC effect. The new pre-driver design can improve the ESD performance of the fully silicided HVT I/O from 500V to 5KV during HBM ESD zapping.

I. INTRODUCTION

The cascode NMOS had been commonly used as the output driver in many circuits such as HVT I/O (Fig. 1) [2] and differential amplifier. For HVT I/O, it often uses the cascode NMOS as the ESD protection device since it has the snapback characteristic. During ESD event, the parasitic npn bipolar transistors of the cascode NMOS [1] can be turned on to discharge the high current.

However, W. R. Anderson had reported that the cascode NMOS during +ESD/Vss zapping event is more vulnerable than the single NMOS [2]. The foundry companies often provide the additional processes, silicide-block and ESD implant, to improve the ESD performance of the cascode NMOS to an acceptable level. Using the silicide-block and ESD implant might be suitable to the HVT I/O. However, the additional masks, processes and I/O cell layout modification will increase the I/O dimension, die size, chip cost and decrease wafer throughput. For differential amplifier, using the silicide-blocked and ESD implant are impossible since they will increase the device parasitic capacitance and resistance, and thus induce noise and power gain loss to an unacceptable level. Currently, the only one solution to improve the ESD performance of differential amplifier is to add the ESD protection device. But, adding an ESD protection device also has the same problem, that is, noise increase and power gain losses, since the pad capacitance is also increased.

In fact, the top gate of cascode NMOS directly connected to Vcc had been found as the root cause of the HVT I/O failed at low voltage ESD zapping [1]. During ESD zapping event, the Vcc (top gate voltage) is pulled-up to a high voltage to turn on the channel of the top NMOS of the cascode NMOS, which results in the current crowded in the channel region and then induces the S/D punch-through (Fig. 2) and degrades the ESD performance of HVT I/O. This phenomenon is called gate voltage-induced current crowding (GVICC) effect. If the GVICC effect can be eliminated, we can deduce that HVT I/O ESD performance should not be degraded.

In this paper, a new design which does not need any additional processes and I/O cell layout modification is proposed to eliminate the GVICC effect for improving the ESD performance of the HVT I/O and differential amplifier.

Fig. 1 The schematic of conventional HVT I/O circuits.

Fig. 2 S/D punch-through occurred on the top NMOS due to GVICC effect.
II. EXPERIMENTS

The devices used in this experiment are 3.3V devices and fabricated by 0.18um CMOS process. Figure 3 shows the layout of the cascode NMOS, which is multi-fingers structure and with 720um total width and 0.4um gate length. All the devices are with CoSi modules and the contact to poly space follows the minimum design rule.

Figure 1 shows the schematic of the conventional HVT I/O circuits composed of a floating well PMOS and a cascode NMOS. Top NMOS’s gate of the cascode NMOS is connected to Vcc directly, and bottom NMOS’s gate of cascode NMOS is connected to the output of pre-driver N.

Figure 4 shows the schematic of the HVT I/O circuits, which can eliminate the GVICC effect during ESD zapping event. It is composed of a floating-well PMOS, a cascode NMOS and an ESD sensing circuit. The ESD sensing circuit is used to detect the ESD signal, and is composed of a diode string and a grounded gate NMOS. Unlike the conventional HVT I/O, the top and bottom gates of the cascode NMOS are connected to the NOR gate “A” and NOR gate “B”, respectively.

III. RESULTS

a. Cascode NMOS and Conventional HVT I/O Circuits

Table 1 shows the It2’s and ESD threshold voltages of a single cascode NMOS (Fig. 5) and conventional HVT I/O (Fig. 1). The only difference between the single cascode NMOS and the cascode NMOS of the HVT I/O circuits is the gate configuration. For the single cascode NMOS, the top gate is floating. For the cascode NMOS of the HVT I/O, the top gate is connected to Vcc directly (Fig. 1). Based on [1], the primary ESD protection device of the HVT I/O is the cascode NMOS. However, we found the It2 and ESD threshold voltages of a single cascode NMOS are much higher than those of HVT I/O.

Figure 6 shows the voltage waveforms of the conventional HVT I/O (Fig. 1) under +500V HBM zapping event. During the snapback region, the pad voltage (drain voltage) and the Vcc (top gate voltage) are nearly 7.2V and 7V, respectively. Because the voltage of the top gate is pulled up to 7V during ESD zapping event, most
currents are limited in the channel region of the top NMOS to result in the HVT I/O circuits failed at low ESD zapping event. This is the gate voltage-induced current crowding (GVICC) effect. However, the coupled gate voltage of the top NMOS for a single cascode NMOS under ESD zapping is below 2V [1]. Without the high gate voltage, the ESD current is not confined in the channel region and can flow the N+ drain junction uniformly. So, the ESD performance of a single cascode NMOS is apparently much higher than that of the HVT I/O.

Table 1

<table>
<thead>
<tr>
<th>Structure</th>
<th>It2 (A)</th>
<th>HBM(KV)</th>
<th>MM(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascode NMOS</td>
<td>2.5</td>
<td>5.0</td>
<td>225</td>
</tr>
<tr>
<td>HVT I/O</td>
<td>0.2</td>
<td>0.5</td>
<td>50</td>
</tr>
</tbody>
</table>

Fig. 6 The voltage waveforms of the HVT I/O in Fig. 3 under +500V HBM zapping event.

b. New HVT I/O Circuits

From above, we can deduce that HVT I/O can be designed as robust as the single cascode NMOS if the GVICC effect can be eliminated. In order to eliminate the GVICC effect, the gate of the top NMOS cannot connect to Vcc directly since the Vcc will be pulled to high voltage during ESD zapping event (Fig. 6). Instead of the top gate connected to Vcc directly, the top gate is connected to the output of a NOR gate (NOR gate “A” in Fig. 4). One input node of NOR gate “A” is connected to Vss, and another input node is connected to the output of the ESD sensing circuit (node S). During normal operation, the top gate voltage is equal to Vcc since the voltages of the two input nodes are 0V. During ESD zapping event, the voltage of the node S is raised up to turn on the transistor of NOR gate “A”, and to pull down the top gate voltage. Based on the same concept, the last stage of the pre-driver N is also modified to a NOR gate (NOR gate “B” in Fig. 4) to ensure that voltage of the bottom gate also can be pulled down during ESD zapping event.

For MOS structure device, its snapback voltage (~7.2V in Fig. 6) is always higher than its normal operation voltage (Vcc). From the voltage difference, whether the circuit is during normal operation or suffered the ESD can be distinguished and can be used to design the ESD sensing circuit. It is well known that diode string is a good voltage clipper. Thus, we can use it to clip the voltage to turn on the transistors of the NOR gates during ESD zapping event and to keep the node S at 0V during normal operation. To satisfy above condition, the number of the diode string should be designed $V_{sp}>V_{Tdio}>V_{cc}$, where $V_{sp}$ is the snapback voltage of the HVT I/O and $V_{Tdio}$ is the threshold-voltage of the diode string. The diode used to build the diode string is the P+/NW diode. Under forwarded bias, it is a pnp bipolar from anode to cathode and P-substrate. So, the diode string becomes a Darlington pair [3] and the $V_{Tdio}$ of the diode string can be shown to be: $V_{Tdio}=\frac{mV_{f}-m(m-1)V_{o}}{kTln(1/q)+1/2}$ (1).

Where $V_{f}$ is turn-on voltage of a diode, $V_{o}=nkTLn(1)/q$, $m$=number of diode string, $\beta$=parasitic pnp bipolar gain.

The number of the diode string used in this ESD sensing circuit is 7. Figure 7 shows the Vout, corresponding to the node S in Fig. 4, versus Vcc at 25°C for ESD sensing circuit. Based on eq. (1), the Vout can be clamped at 0V by the diode string if the Vcc is $\leq V_{Tdio}$ (~4V). And, the Vout is equal to Vcc–$V_{Tdio}$ if the Vcc is $>V_{Tdio}$.

Figure 8 shows the DC characteristics of the top gate, bottom gate (pre-driver N) and pad versus Vcc for new designed HVT I/O (Fig. 4). As we set the two input nodes of the pre-driver (OEN and Signal) as 0V and sweep the Vcc, we can find the voltages of the top gate and the bottom gate are equal to Vcc until the Vcc increased to 5.2V. If the Vcc is higher than 5.2V, the transistors of the two NOR gates can be turned on since the voltage of the node S is raised up to 0.6V (Fig. 7) which is higher than the Vt of 3.3V NMOS. So, both the voltages (top and the bottom gates) can be pulled down to 0V. It proves that the function of this new schematic is the same as the conventional HVT I/O during normal operation for 3.3V Vcc. And, the voltages of the top gate and bottom gate all can be pulled down.
when the ESD sensing circuit detects an abnormal signal in Vcc.

Figure 9 shows the voltage waveforms of the HVT I/O with the ESD sensing circuit during +500V HBM/Vss zapping event. The snapback voltage (pad voltage) is higher than 5V, and the voltages of the top gate and bottom gate all can be clamped below 2V. This proves that the new design in Fig. 4 can pull down the voltages of the top gate and the bottom gate of the cascode NMOS of the HVT I/O under ESD zapping event. So, it can eliminate the GVICC effect.

Without the GVICC effect, the current flows can uniformly distribute in the cascode NMOS as the HVT I/O under ESD zapping event. It implies the new designed HVT I/O circuit has the larger effective area (\(A_{\text{eff}}\)) for discharging ESD current. For a given stress condition (\(I=\text{const}\)), the stress current density (\(J=I/A_{\text{eff}}\)) of this new designed HVT I/O circuit should be smaller than that of the conventional HVT I/O circuit. By comparing the test results of the Fig. 6 and Fig. 9, we can find the \(V_{sp}\) (~5V) of the new designed HVT I/O circuit is smaller than the \(V_{sp}\) (~7V) of the conventional HVT I/O circuit. The ESD sensing circuit does not only affect the current distribution of the cascode NMOS but also affect the \(V_{sp}\) of the HVT I/O circuit. It implies that the power generation (\(P=J\times V_{sp}\)) of the HVT I/O circuit under the ESD zapping can be decreased significantly if the GVICC effect is eliminated. So, the ESD performance of the HVT I/O can be improved. Without any additional process and I/O cell layout modification, the \(I_{\text{t2}}\) of this new designed HVT I/O circuit can be increased from 200mA to 3A. The HBM failure threshold can be improved from 0.5KV to 5KV, and the MM failure threshold can be improved from 50V to 250V.

IV. CONCLUSION

In this paper, we have demonstrated the gate potential induced by ESD can affect the I/O ESD performance significantly. This implies the I/O ESD performance not only depends on the layout of the I/O cell but also depends on the internal circuit. So, during ESD zapping event, the gate potential of the fingers used as the driver should be pulled to 0V to prevent the current crowded in the channel region. In addition, a new design is also demonstrated to eliminate the GVICC effect of the HVT I/O during ESD event. This new pre-driver design for HVT I/O can improve the HVT I/O ESD performance significantly and without increasing additional process and I/O cell layout modification.

![Image](https://example.com/image1.png)

**Fig. 7 a. The ESD sensing circuit in Fig. 4, b. The Vout (S in Fig.4) vs. Vcc for ESD sensing circuit.**

![Image](https://example.com/image2.png)

**Fig. 8 The DC characteristics of HVT I/O in Fig. 4.**

![Image](https://example.com/image3.png)

**Fig. 9 The voltage waveforms of HVT I/O circuit in Fig. 4.**

REFERENCES