ABSTRACT
We investigate techniques to design 45nm minimum-energy subthreshold CMOS circuits under timing constraints, considering the practical case of an 8-bit multiplier. We first show that technology flavor and $V_t$ selections shift minimum-energy point to different operating frequencies, thereby enabling minimum energy in either low- or mid-performance applications. However, we demonstrate that independent dual-$V_t$ assignment to save leakage in non-critical paths is not feasible. We then show that reverse adaptive body biasing (ABB) is potentially more efficient to compensate for global process/temperature variations than adaptive voltage scaling and forward ABB. Nevertheless, its practical efficiency is limited by the affordable $V_{dd}$ range and the value of the body-effect coefficient.

Categories and Subject Descriptors
B.7.1 [Hardware]: Types and Design Styles; B.8.2 [Hardware]: Performance Analysis and Design Aids.

General Terms
Design, performance.

Keywords
CMOS digital integrated circuits, adaptive circuits, subthreshold logic, ultra-low power, variability.

1. INTRODUCTION
Subthreshold design is a vibrant research direction for ultra-low-power applications with loose speed requirements such as biomedical devices, sensor networks and RFID tags. Depending on the target frequency $f_{target}$ of the application and resulting minimum $V_{dd}$ for meeting the subsequent timing constraint, it is shown in [1] that there is an optimum technology node for minimizing energy per operation $E_{op}$. Generally speaking, the authors show that nanometer technologies are more efficient for mid-performance (5-500 MHz) applications thanks to reduced switching energy $E_{sw}$ (lower capacitance and minimum $V_{dd}$), while older technologies fit low-performance (50 kHz-5 MHz) applications thanks to reduced leakage energy $E_{leak}$. This is confirmed in Fig. 1 for the practical case of an 8-bit RCA multiplier (logic depth is 23). Spice simulations are carried out in general-purpose (GP) bulk CMOS technologies from an industrial foundry at 130 and 45 nm nodes to extract (a) the minimum $V_{dd}$ for meeting the timing constraint, and (b) corresponding $E_{op}$.

In these simulations, local variability is considered through Monte-Carlo statistical extraction of the minimum $V_{dd}$ that ensures 99.9% yield in both functionality (method from [2]) and timing. When migrating to 45 nm node, the frequency $f_{min}$ of minimum-energy point $E_{min}$ resulting from a balance between $E_{sw}$ and $E_{leak}$ is shifted towards higher $f_{target}$. Moreover, the reduced noise margins from large local variability imply an increase in the functional-yield limit on $V_{dd}$, which results in a further $E_{leak}$ increase [3]. For the considered multiplier, 130 nm technology is more energy-efficient for applications with $f_{target}$ below 10 MHz.

Figure 1: Minimum $V_{dd}$ (a) and resulting energy per operation $E_{op}$ (b) of an 8-bit multiplier under functional- and timing-yield constraints.
tion of this interest, we saw in the last past months a growing number of subthreshold circuits implemented in 65 and even 45 nm technologies [4, 5]. Therefore, in this paper, we address design techniques for minimizing energy consumption of timing-constrained sub/near-threshold circuits in nanometer technologies, for a wide $f_{\text{target}}$ range i.e. for either low- or mid-performance applications. We consider the practical case of the 8-bit RCA multiplier at 45 nm node but the conclusions can easily be transposed to 65 nm node and/or to any combinatorial circuit. In Section 2, we consider the interest of technology flavor and $V_t$ selections. We then address adaptive techniques for compensating global process and temperature variations in Section 3.

In Fig. 1, let us point out that $E_{\text{min}}$ level is 30% higher in 45 than in 130 nm technology. We showed in [6] that it comes from the increased DIBL, gate leakage and local variability in nanometer technologies. In that paper, we further proposed guidelines to select optimum 45 nm MOSFETs within a technology flavor, for minimizing $E_{\text{min}}$ regardless of the timing constraints. Relying on those guidelines, the resulting optimum MOSFETs from each technology flavor can then be used as a starting point for the flavor selection proposed in next section. However, for the sake of generality, we restrict the discussion to baseline devices, as offered by the foundry in its standard-cell libraries.

### 2. TECHNOLOGY SELECTION

Since 90/65 nm node, technologies often come in various flavors to achieve different speed/power trade-offs. The industrial 45 nm technology we consider features 2 flavors: a thin-oxide mid-$V_t$ short-channel flavor denominated as general-purpose (GP) and a low-power (LP) flavor with thick-oxide high-$V_t$ mid-channel devices. Both flavors are dual-$V_t$ technologies, i.e. with std-$V_t$ and high-$V_t$ devices. Main MOSFET parameters are given in Table 1. Let us see the impact of these flavors on the multiplier energy consumption.

#### 2.1 Technology flavor selection

Simulated minimum $V_{dd}$ for meeting 99.9% functional-yield and timing-yield constraints of the multiplier is plotted in Fig. 2 (a) for both GP and LP flavors. As a consequence of its higher $V_t$ and thus lower subthreshold $I_{\text{on}}$, LP flavor features an increased delay at a given $V_{dd}$ and thus requires a higher $V_{dd}$ for meeting the timing constraint. Minimum $V_{dd}$ for meeting functional-yield constraint is comparable in GP and LP technologies. As a result, the boundary between robustness-constrained and timing-constrained frequency regions is shifted to lower frequencies for LP flavor.

Corresponding energy per operation $E_{\text{op}}$ of the multiplier is plotted in Fig. 2 (b). The lower subthreshold current of LP flavor implies a similar shift of the $E_{\text{op}}$ curve to lower frequencies. Thanks to its lower minimum $V_{dd}$ for meeting the timing constraint, GP flavor features lower $E_{\text{op}}$ for target frequencies above 8 MHz, where switching energy dominates, as the switched capacitance is roughly equivalent between GP and LP flavors. Nevertheless, $E_{\text{op}}$ in GP flavor dramatically increases for lower $f_{\text{target}}$ as the circuit becomes dominated by leakage energy. As a result, LP flavor features the lowest $E_{\text{op}}$ for $f_{\text{target}}$ below 8 MHz. This shows that there is an optimum technology flavor depending on the target frequency of the considered application.

#### 2.2 Global $V_t$ selection

As both flavors are dual-$V_t$ technologies, minimum $V_{dd}$ and corresponding $E_{\text{op}}$ for the multiplier have been simulated for high-$V_t$ devices and are plotted in Fig. 2 (dashed lines). A global $V_t$ selection, common to all logic gates, implies a further shift of the $E_{\text{op}}$ curve vs. $f_{\text{target}}$. It thus offers a finer granularity for performance tuning to make minimum-energy point of the multiplier correspond to the target frequency of the application, i.e. to make $f_{\text{min}}$ meet $f_{\text{target}}$. Combining technology flavor and global $V_t$ selection by considering the minimum of the four $E_{\text{op}}$ curves yields an optimum $E_{\text{op}}$ envelope. Technology versatility is thus a powerful tool to achieve ultra-low energy per operation for any application with a target frequency between 10 kHz and 100 MHz.

#### 2.3 Independent dual-$V_t$ assignment

Global $V_t$ selection enables the matching of $f_{\text{min}}$ with $f_{\text{target}}$. However, it does not bring significant improvement in minimum-energy level $E_{\text{min}}$ of the multiplier because the leakage current saved by using high-$V_t$ devices is lost in terms of delay and thus minimum $V_{dd}$ for meeting the timing constraint. In dual-$V_t$ technology it is also possible to assign the device $V_t$ to each logic gate independently. Such independent dual-$V_t$ assignment is commonly used in high-speed low-power circuits: assigning high-$V_t$ devices to non-critical paths saves leakage, while keeping std-$V_t$ devices in critical paths preserves speed performances [7]. Let us investigate dual-$V_t$ assignment for nanometer subthreshold circuits.

### Table 1: MOSFET parameters in the considered industrial technologies

<table>
<thead>
<tr>
<th>Tech. node flavor</th>
<th>$L_g$ [nm]</th>
<th>$T_{ox}$ [nm]</th>
<th>$V_{dd,nom}$ [V]</th>
<th>$V_{t,nom}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 GP</td>
<td>120</td>
<td>2.0</td>
<td>1.2</td>
<td>0.45/0.61</td>
</tr>
<tr>
<td>45 GP</td>
<td>35</td>
<td>1.2</td>
<td>0.9</td>
<td>0.41/0.55</td>
</tr>
<tr>
<td>45 LP</td>
<td>42</td>
<td>1.7</td>
<td>1.1</td>
<td>0.55/0.68</td>
</tr>
</tbody>
</table>

### Figure 2: Comparison of 45 nm GP and LP flavors.

The LP flavor shifts the multiplier $E_{\text{op}}$ curve to lower $f_{\text{target}}$. Combining flavor and $V_t$ selections enables low energy consumption for a wide $f_{\text{target}}$ range.
whereas at subthreshold 0.3V

At nominal 1.1V $V_{dd}$, the high-$V_t$ multiplier is 60% slower whereas at subthreshold 0.3V $V_{dd}$, it is 7× slower. This will clearly limit the use of independent dual-$V_t$ assignment technique as high-$V_t$ devices can only be assigned to paths with a logic depth far smaller than the critical path. Moreover, short paths feature higher variability due to local device variations such as random dopant fluctuations (RDF) because local variability is less averaged between logic gates. As local variability cannot be compensated, it may further decrease the maximum number of logic gates in high-$V_t$ paths.

In order to quantify that, we need a model of variability vs. the logic depth i.e. the number of stages $N$ in the logic path. The delay of the path is the sum of the delay of all its logic gates, which are proportional to $C_L V_{dd}/I_{on}$. At nominal $V_{dd}$, $I_{on}$ and thus $T_{del}$ can be modeled by a normal distribution because of their alpha-power dependence on normally-distributed $V_t$. The sum of normally-distributed $T_{del}$ is another normal distribution with the standard deviation averaged in $1/\sqrt{N}$ [8]. As shown in Fig. 4 (a), there is a very good agreement between this $1/\sqrt{N}$ law and Spice simulations of N-stage FO4 inverter chain.

In subthreshold regime, $I_{on}$ is a subthreshold current and its distribution thus follows a lognormal law because of its exponential dependence on normally-distributed $V_t$. In [9], the delay variability of a path made of subthreshold logic gates is shown to follow this law:

$$\sigma(t_{\text{del}}) = \sqrt{\ln \left(1 + \frac{1}{N}(10^{23} - 1)\right)}.$$  \hspace{1cm} (1)

where $t = \sigma_{Vt}/S$ with $S$ is the subthreshold swing. As shown in Fig. 4 (b), Spice simulations closely match this law.

Let us study the efficiency of dual-$V_t$ assignment for nanometer subthreshold circuits by considering the following case: a subthreshold circuit with the 8-bit RCA benchmark multiplier as a component. Std-$V_t$ devices are assigned to all logic gates, by default. As the multiplier features a large logic depth (23 complex gates), it is likely that it will contain the critical path of the circuit. Let us see how short a non-critical path should be to assign it high-$V_t$ devices without making it become critical, i.e. without raising its delay above the multiplier delay. To do so, we compute the typical delay of an $N$-stage high-$V_t$ FO4 inverter chain from simulation of a 10-stage chain, relying on proportionality of the typical delay vs. $N$ (verified by simulation). We then compare this typical delay to the delay of the std-$V_t$ multiplier under various supply voltages from 1.1V down to 0.3V. We can thus predict how many high-$V_t$ FO4 inverters will result in a typical delay higher than the multiplier critical path. The result is shown in Fig. 5 (dashed line). At nominal 1.1V $V_{dd}$, a chain of 32 FO4 inverters has a delay just below the multiplier delay. However, when scaling $V_{dd}$ down to 0.3V, the maximum number of inverters in the path for high-$V_t$ assignment is reduced to 7.

Let us now consider the impact of local variability. From the aforementioned delay variability models, we predict the $3\sigma$ worst-case delay of an $N$-stage FO4 high-$V_t$ inverter chain and compare it to the simulated $3\sigma$ worst-case delay of the multiplier at various supply voltages. Fig. 5 shows the calculated maximum number of FO4 inverters in a high-$V_t$ path to keep its worst-case delay below the worst-case delay of the multiplier critical path. The impact of variability on nominal $V_{dd}$ operation is important: it reduces the maximum log depth of high-$V_t$ paths to 19 FO4 inverters, and the impact on subthreshold operation is disastrous: high-$V_t$ devices can only be assigned to paths with 2 FO4 inverters. This clearly demonstrates the inefficiency of individual dual-$V_t$ assignment in nanometer subthreshold circuits as high-$V_t$ devices can only be assigned to very short paths.
Figure 6: Impact of global process and temperature variations on (a) minimum $V_{dd}$ and (b) energy per operation. In (b), solid lines represent the operation at the actual minimum $V_{dd}$ i.e. without $V_{dd}$ margin while dashed lines represent operation at the worst-case minimum $V_{dd}$ from SS corner at -15°C.

2.4 Impact of global corners

As shown in Fig. 2 (b) by taking the minimum of the four $E_{op}$ curves, the versatility of the technology provides a high potential for minimizing $E_{op}$ for a wide frequency range by correct technology flavor and $V_{t}$ selections. However, there are several phenomena that may jeopardize the choice of the optimum flavor/$V_{t}$. Indeed, global process and temperature variations as well as aging effects imply $V_{t}$ variations. The phenomena that increase $V_{t}$, such as an SS (slow NMOS, slow PMOS) process corner, a temperature lowering or negative-bias temperature instability (NBTI) in PMOS devices, increase circuit delay and might thus imply timing violations. Design margins on $V_{dd}$, for instance, are thus required to avoid it. The phenomena that reduce $V_{t}$, such as FF (fast NMOS, fast PMOS) process corner or a temperature rise, reduce the delay but increases leakages. This is illustrated in Fig. 6 (a) where minimum $V_{dd}$ of the multiplier for meeting both the functional- and timing-margin constraints is plotted for SS corner at -15°C, SS, TT and FF corners at 25°C and for FF corner at 55°C (again considering local variability with Monte-Carlo simulations at each corner). Minimum $V_{dd}$ is the highest for SS corner at -15°C, which is thus the worst-case corner regarding speed.

Fig. 6 (b) shows corresponding energy consumption of the multiplier for the same process/temperature corners. $E_{op}$ is plotted in dashed lines when considering design margins on $V_{dd}$, i.e. when operating at the worst-case $V_{dd}$ (i.e. minimum $V_{dd}$ of SS corner at -15°C). For comparison purpose, $E_{op}$ for TT corner at 25°C is also plotted in solid line without design margins i.e. when considering the actual minimum $V_{dd}$ of this corner represented in Fig. 6 (a). This shows that process/temperature variations shift the minimum-energy point to different application frequencies. Moreover, design margins introduce large energy overheads. Let us assume that we were able to select a technology flavor and a $V_{t}$ value that make minimum-energy point meet the target frequency i.e. $f_{min} = f_{target}$ for TT corner at 25°C, which is 340 kHz in our case. Under this condition, the design margin on $V_{dd}$ introduces 50% and 70% energy overheads as compared to typical minimum energy $E_{min,typ}$ due to increased leakage for TT and FF corners at 25°C, respectively. Furthermore, a temperature rise to 55°C implies an energy overhead up to 230% at FF corner. As leakage energy suffers from the highest variability, Fig. 6 shows that operating at a higher frequency with dominating $E_{leak}$ enables lower worst-case energy. The corresponding worst-case minimum $E_{min,WC}$ energy has a 100% energy overhead. This worst-case energy curve has thus to be taken into account when making the $V_{t}$/$V_{dd}$ selection as proposed in previous sections. Moreover, circuit adaptation can be used for avoiding the $E_{leak}$ overhead associated to the worst-case FF corner at 55°C. Such adaptive techniques are investigated in next section.

3. CIRCUIT ADAPTATION

Traditionally, digital circuits are designed with the target to meet the timing constraints at the worst-case process, voltage and temperature corner. As shown in previous section, a design margin on $V_{dd}$ might imply more than 200% energy overhead at worst-case corner for energy. As these variations are global, they can be compensated by adaptive techniques in order to avoid taking large design margins on $V_{dd}$ to handle worst-case conditions. Main techniques for adaptation of subthreshold circuits are adaptive supply voltage scaling (AVS) and adaptive body biasing (ABB) [10,11]. In this section, we first analyze the impact of body biasing on energy in nanometer subthreshold circuits and then compare the use of AVS and ABB for circuit adaptation, considering the 8-bit RCA multiplier in 45 nm LP technology. We finally extend this investigation with a discussion on the efficiency of ABB between technology flavors.

3.1 Impact of body bias on energy

Body biasing implies a $V_{t}$ shift and consequently an exponential subthreshold current modification. This in turn impacts the delay and leakage of subthreshold circuits. As shown in Fig. 7, the delay modification results in a shift of the minimum $V_{dd}$ for meeting the timing constraint to higher (resp. lower) $V_{dd}$ values for reverse (resp. forward) body bias, similarly to $V_{t}$ selection as explained in Section 2.2. With a 1V BB range (-0.6 to 0.4V), energy can be kept at $E_{min}$ for a wide $f_{target}$ range (from 0.1x$f_{min}$ to 0.1x$f_{min}$, with $f_{min} = 340$ kHz). This shows that BB is a powerful technique for circuit adaptation to shift minimum-energy point by fine tuning of $f_{min}$. The extracted BB impact on $f_{min}$ is 60x$V_{t}$. Interestingly, notice that the optimum supply voltage $V_{min}$ of minimum-energy point is quite insensitive to the body voltage $V_{BB}$. This means that adaptation can be performed through ABB with fixed $V_{dd}$.

We also observe in Fig. 7 (b) a modification of $E_{min}$ level with $V_{BB}$. It is shown in [12] that $E_{min}$ is proportional to the mean load capacitance multiplied by the square of the subthreshold swing, $C_{L}V_{t}^2$. The application of a forward BB increases $E_{min}$ first by $S$ degradation and $C_{L}$ increase (through intrinsic gate capacitance in subthreshold regime) due to a reduction of the channel-depletion thickness. Then, exponential increase of drain-to-substrate junction leakage further increases $E_{min}$ level. A $V_{BB}$ of +0.5V (not represented in Fig. 7) leads to 50% increase in $E_{min}$ level. Adaptation through forward ABB thus comes with $E_{min}$ penalty.
loop, which becomes increasingly frequent in both low-run time by using a critical path replica in a delay-locked factured chips. In the case of process, temperature and aging frequencies different from maximum. This can occur in two cases. Case 1 - deviation from model because of modeling errors, global process/temperature variations or device aging. In the case of a modeling error, post-Silicon compensation can be achieved at test time by application of static compensation parameters (Vdd for AVS scheme or VBB for ABB scheme) extracted from measurement of a few manufactured chips. In the case of process, temperature and aging variations, the compensation should preferably be done at run time by using a critical path replica in a delay-locked loop [13], which becomes increasingly frequent in both low-power and high-performance nanometer circuits.

Case 2 - adaptation to dynamic workload if the target ftarget varies at run time. For an embedded microprocessor, this could correspond to a low-performance mode at 100 kHz and a mid-performance mode at 10 MHz for instance. In this case, run-time adaptation can be achieved with reconfiguration parameters (ftask = ftarget and Vdd/VBB) statically encoded in a power-state look-up table.

Next experiment addresses both cases by computation of the Eop for a wide frequency range centered on fmin with AVS and ABB schemes, which is similar to an actual fmin that differs from ftarget. First, Fig. 8 (a) shows the minimum Vdd for the 8-bit multiplier to support target application frequencies different from fmin. A 200mV Vdd range between 0.25 and 0.45V can accommodate two decades of ftarget variations. Corresponding Eop in Fig. 8 (b) follows the usual evolution, being dominated by Esub for ftarget > fmin and by Eleak for ftarget < fmin. At ftarget = 0.1 fmin, there is a 70% energy overhead with AVS technique. Secondly, when considering a fixed Vdd = Vmin = 0.35V, minimum VBB to support ftarget is represented in Fig. 8 (a) and shows that two decades ftarget variations can be accommodated by a 1.1V VBB range between -0.6 and 0.5V.

3.2 ABB vs. AVS for circuit adaptation

As shown in Fig. 2, once the technology flavor and device Vt are selected, minimum-energy operation can only be reached for one particular ftarget. Adaptation is required when ftarget does not match the fmin frequency of minimum-energy point. This can occur in two cases.

Case 1 - deviation from model because of modeling errors, global process/temperature variations or device aging. In the case of a modeling error, post-Silicon compensation can be achieved at test time by application of static compensation parameters (Vdd for AVS scheme or VBB for ABB scheme) extracted from measurement of a few manufactured chips. In the case of process, temperature and aging variations, the compensation should preferably be done at run time by using a critical path replica in a delay-locked loop [13], which becomes increasingly frequent in both low-power and high-performance nanometer circuits.

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The impact of ABB on Eop shown in Fig. 8 (b) is comparable to AVS at high frequencies. However, at low frequencies, reverse ABB is much more efficient as it keeps Eop at the Emin level. This experiment shows that reverse ABB is more energy-efficient than forward ABB in 45 nm sub-threshold circuits because forward ABB suffers from Emin increase. Furthermore, reverse ABB is potentially more efficient than AVS. Theoretically, designers should thus make the circuit operate at minimum Vdd of worst-case corner for speed (SS corner at low temperature) and rely on reverse ABB to benefit from a potential positive timing slack for saving extra leakage energy.

3.3 Discussion

Let us now see how the technology selection proposed in Section 2 affects the use of reverse ABB. To do so, Fig. 9 plots the process/temperature-induced Esub and Eleak variability of the multiplier (ratio between worst-case FF/55°C and best-case SS/-15°C corners) in both 45 nm LP and GP flavors, as compared to 130 nm GP technology. This first shows that Esub variability is pretty much stable with technology scaling, whereas Eleak variability is reduced in 45 nm technology. This comes from the increasing proportion of gate leakage in nanometer technologies, which is more stable vs. temperature than subthreshold leakage.

Secondly, Eleak variability is compared when applying reverse ABB with a limited VBB range. Indeed, supplying +1V and -1V or higher bias voltages for reverse ABB to a chip operating with 0.3V Vdd is a fanciful target, especially for low-cost small-form-factor applications such as RFID tags or biomedical devices, which cannot rely on multiple off-chip voltage sources. Fig. 9 thus shows the Eleak reduction, when considering a maximum affordable VBB of -0.5V. In 45 nm GP flavor, the low body-effect coefficient (γ = 85mV/V) due to thin gate oxide and short gate length limits the Eleak reduction from reverse ABB to a factor 2 only. However, in LP flavor, the body-effect coefficient is larger (γ = 120mV/V) and worst-case Eleak with -0.5V maximum VBB is reduced by a factor 6.6. This leads to a worst-
case $E_{\text{leak}}$ with -0.5V reverse ABB scheme in 45nm LP flavor 7.4× higher than best-case $E_{\text{leak}}$ while in GP flavor it is 24× and 54× higher at 130 and 45 nm nodes, respectively.

This shows that the efficiency of reverse ABB is mainly limited by two factors: the affordable $V_{BB}$ range and the body-effect coefficient. LP flavor in 45nm technology is more adapted to reverse ABB sub/near-threshold circuits than GP flavor, thanks to higher body-effect coefficient. As mid-performance applications require a GP flavor to operate at the minimum-energy point under timing constraints, new device paradigms or architectures are needed for mid-performance sub/near-threshold nanometer circuits that either bring lower sensitivity against variations or higher capability of $V_i$ adaptation.

Finally notice that at 32 nm node high band-to-band tunneling, although reduced at low $V_{dd}$, might further limit the efficiency of reverse ABB for subthreshold circuits. Moreover, at that node even in LP flavor, the reduced body-effect coefficient might not be sufficient.

4. CONCLUSION

In this paper, we investigated techniques to design 45nm subthreshold circuits operating at minimum-energy point under timing constraints across wide process and temperature variations. Based on the practical case of an 8-bit multiplier, we first showed that selecting the technology flavor and device variations. Based on the practical case of an 8-bit multiplier, we first showed that selecting the technology flavor and device variations. Based on the practical case of an 8-bit multiplier, we first showed that selecting the technology flavor and device variations. Based on the practical case of an 8-bit multiplier, we first showed that selecting the technology flavor and
dered the efficiency of ABB.

We observed that global process/temperature variations may imply a wrong frequency estimation of minimum-energy point and thus an inappropriate flavor selection, leading to energy overhead higher than 200% at the worst-case corner for energy. We then showed that adaptive body biasing (ABB) is potentially more efficient than adaptive supply voltage scaling, to compensate for this frequency mismatch. However, this is only true for reverse ABB as forward ABB increases minimum-energy level due to subthreshold swing degradation, increase of intrinsic gate capacitance and junction leakage. When making the flavor/$V_i$ selection, designers thus have to ensure that the circuit relying on reverse ABB meets the timing constraint at the worst-case process/temperature corner for speed (SS process at low temperature). Reverse ABB can then used to dynamically increase $V_i$ for limiting potential extra leakages in case of a positive timing slack. At 45 nm node, we point out that reverse ABB is only efficient in LP technology flavor because of vanishing body-bias coefficient in GP flavor. This limits the interest of nanometer GP flavor in bulk technology for mid-performance nanometer subthreshold circuits and reemphasizes the need for a technology with low sensitivity against process and temperature variations.

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6. REFERENCES


