Design constraints for low distortion OTA's in on-chip analog front-ends

This paper discusses design constraints for low distortion Operational Transconductance Amplifiers (OTAs) on integrated analog front ends. It also compares traditional OTA topologies and proposes a new OTA showing significant reduction on distortion for wideband applications, the comparison is presented on a 0.35µm CMOS process. The proposed OTA is designed for on-chip analog front ends for radiation gamma detectors on a 130nm CMOS process.

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Design Constraints for Low Distortion OTA’s in On-Chip Analog Front-Ends

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Abstract—This paper discusses design constraints for low distortion Operational Transconductance Amplifiers (OTAs) on integrated analog front ends. It also compares traditional OTA topologies and proposes a new OTA showing significant reduction on distortion for wideband applications, the comparison is presented on a 0.35µm CMOS process. The proposed OTA is designed for on-chip analog front ends for radiation gamma detectors on a 130nm CMOS process.

Index Terms—Operational Transconductance Amplifiers, Analog Front-End, Gamma-Cameras.

I. INTRODUCTION

Operational Amplifiers are elementary blocks for analog signal processing systems. For on-chip systems, the Operational Transconductance Amplifier (OTA) is the most compatible configuration with standard CMOS process. Important specifications such as DC gain, bandwidth, slew rate and power consumption must find a good trade-off to increase benefits for certain applications. Among these parameters, signal distortion is critical when processing deals with high-level signal swings at OTA’s output. For instance, in Analog to Digital Converters (ADCs) signal swings constraint the effective resolution, as distortion from OTAs might reduce the SNR at internal nodes [1]. Therefore, distortion related to signal swings (clipping distortion) is a very important specification which must be considered when designing OTAs.

To limit distortion on an OTA, it is desirable to maintain transistors on the same region to avoid non linearity. Even if there are several techniques to reduce distortion such as multi-phase post processing, the price for post processing is considerable compared to the overall benefit [2].

This paper presents a distortion comparison between OTA topologies and presents the design of a low distortion OTA in a standard Bulk CMOS process. The presented amplifier was designed for an analog front-end in a Switched-Capacitor based circuit to detect scintillation events on Position Sensitive Photomultiplier Tubes Matrix (PSPMTs) for gamma cameras having Medical applications (previously reported [3]). The paper is organized as follows: Section II presents a comparison for typical OTA topologies and their distortion performance, Sections III and IV present the proposed OTA topology to be used in a gamma camera front end (designed on a CMOS 130nm process). Finally Section V draws conclusions.

II. DISTORTION FOR TYPICAL OTA TOPOLOGIES.

For analog signal processing, distortion can be classified as linear and non linear. Linear distortion is related to filtering process on analog signals and is out of the scope of this work. On the other hand, non linear distortion is related to circuit’s deviation response rising from a change on signal transference (possibly as a result from a change on device region of operation). The amplifier’s non linearity can be also viewed as the change of transconductance as function of the input signal which means that output signals are saturated at a certain input amplitude level (it is typically known as clipping distortion). Last but not least, frequency response also affects the OTA non linear response. This section presents a comparison between distortion levels for three typical OTA topologies.

Fig. 1 shows schematics of a Mirrored, Folded Cascode and Symmetrically Compensated Folded Cascode [4] OTAs. The mirrored amplifier is a two stages amplifier whose frequency response does not require a compensation network. For this amplifier, the differential pair has diode connected transistors as loads that transfer signal by means of a current mirror (having both an AC a DC paths). The advantage for this circuit is the high output swing, as output stage transistors need only one overdrive to maintain operation on saturation region. On the other hand, folded cascode amplifier require four piled transistors at the output stage (shown in Fig. 1). Even if folded cascode amplifiers are compatible with low voltage bias schemes, the output swing is limited which gives an important design consideration for low distortion applications. Another limitation for this amplifier is the limited input dynamic range as for both, mirrored and folded cascode, \( V_{in} \geq V_{dsat} + V_{gs} \) on the differential pair. Alternatively, the symmetrically compensated amplifier has a complementary input as is also shown in Fig. 1 that not only increases input dynamic range but also sets a class AB configuration at OTA’s output. However, the drawback for symmetrically compensated amplifier is the output nodes limited swing.

From previous qualitative analysis it is possible to argue that mirrored amplifiers are a good choice for low distortion topologies. To characterize distortion on these amplifiers this work presents a total harmonic distortion test from an AC
analysis at transistor level design. For comparison purposes
the three amplifiers were designed in a CMOS 0.35µm process
and total harmonic distortion is estimated from the AC analysis
as $THD = \frac{1}{R_1} \sqrt{\sum_{m=2}^{m=0} R_m^2 \times 100\%}$, where $R_m$ are the $m$-th
components, and $R_1$ is the fundamental component.

Fig. 2 shows AC distortion analysis for the aforementioned
OTA topologies. Bias voltages are set to 3.3 V and output
dynamic ranges (obtained from DC sweep) are: 2.6 V for
mirrored, 0.75 V for folded cascade and 1.2 V for symmetri-
cally compensated. Therefore, output dynamic ranges are
different for every topology. As expected from this analysis,
symmetrically compensated and folded cascade amplifiers
present distortion values near to −10dB whereas mirrored
amplifier presents low distortion levels for wide spectrum
(−20dB). Note that even if output dynamic range for folded
cascade is almost twice the folded cascade, distortion levels
are on the same order of magnitude. This let us to conclude
that the output dynamic ranges can give a notion for the
clipping distortion but most important non linear distortion
sources give rise from piled transistors on first stage.

III. DESIGN OF LOW DISTORTION TWO STAGES OTA

For low distortion OTA design it is desirable to use an
output stage having only two transistors at the output stage.
Using this strategy it is possible to ensure maximum swing
at the output nodes, and therefore, to reduce distortion from
amplitude clipping. A direct approach is to use a two stages
amplifier possibly with a preamplifier stage and a class AB output for second stage as shown in Fig 3. \(M_{21}, M_{23}\) compose the second stage and for brevity only the pre-amplifier transistors \(M_{4}, M_{7}, M_{11}, M_{14}\) are shown. A disadvantage for this approach (from now, called SCID) is the limited quiescent current control at the output stage which is not beneficial for process, voltage and temperature variations (PVT). Circuit analysis on the half schematic in Fig. 3 yields an input to output transference:

\[
\frac{V_o}{V_{in}} \approx \frac{g_{m_{2}} g_{m_{21}}}{g_o} \left( 1 + s \frac{C_{p1}}{g_{m_{2}}} \right) \left( 1 + s \frac{2C_{p2}}{g_{m_{2}}} \right) \left( sC_L + g_x \right)
\]

where \(g_o \approx \frac{(g_{ds10}(g_{ds1} + g_{ds13})/g_{m10})}{g_{m3}}\), \(C_{p1}, C_{p2}\) are parasitic transistors at the preamplifier [4] and \(C_x\) is the first stage output parasitic capacitance. As shown on eqn. (1) the additional stage adds an extra pole if transconductances from input and output stages \(g_{m_{21}}\) are not several times different between each other. A compensation scheme is mandatory and this limits bandwidth on frequency response.

To avoid this drawback, this work proposes the Modified Symmetrically Compensated (SCMOD) configuration show in Fig. 4. The scheme is composed by two preamplifier compensated stages (whose differential pair is \(M_{1,2}, M_{12,13}\) respectively). To reduce output nodea non linearity, the stage is converted to a mirrored scheme by connecting a current mirror as load, making an AC path for the output node. The current mirror is on saturation region as long as the output node is at a higher value than an overdrive \((V_{gs10,11} - V_{in})\). A circuit analysis of the proposed scheme yields:

\[
\frac{V_o}{V_{in}}(s) = \frac{g_{ds1}(C_L)(s + z_1)}{C_{gd1}C_{gd3}(s + p_1)(s + p_2)}
\]

a zero and two poles are located respectively at:

\[
z_1 = \frac{(g_{ds3} + g_{ms})}{C_{gd3} + C_{L}}
\]

\[
p_{1,2} = \frac{a \pm \sqrt{a^2 - 4b}}{2}
\]

Figure 5 depicts the frequency response of the proposed amplifier. The amplifier has a unity gain frequency response \(\omega_0 = 228\text{MHz}\) a DC gain \(A_v = 44.7\text{dB}\) and a phase margin of 47deg. Contrary to the SCID topology, the proposed circuit maintains control on the output stage quiescent currents to enhance PVT tolerance.

**IV. DISTORTION CHARACTERIZATION**

To compare distortion circuit performance, fully differential characterization with typical Common Feedback Configurations were used. To ensure the circuit is being tested under similar conditions, the fully differential amplifiers were tested on an analog inverter stage similar to Switched-Capacitor analog front end for PSPMTs tubes which is the final application [3]. Fig. 6 shows frequency responses comparison when using symmetrically compensated OTA, SCID and the proposed SCMOD as an analog inverter. The SCMOD presents lower distortion levels for all frequencies (starting from \(-78\text{dB}\) at DC). For high frequencies the SCMOD OTA maintains low
distortion levels, $-33\text{dB} \pm 1\text{MHz}$. Results show values of $\approx -10\text{dB} \pm 1\text{MHz}$ for the SCID and symmetrically compensated OTA respectively. Table I resumes circuit performances for every OTA analyzed in this work. Note the SCID amplifier presents high gain and bandwidth product ($GBW$) but at the expense of very high power consumption ($\text{Power Cons.}$), not practical for portable applications. Proposed SCMOD OTA has the lowest distortion level but presenting low DC gain. For $GBW$ product, SCMOD is comparable to the symmetrically compensated amplifier. Being SCMOD the best configuration for low distortion applications, it was designed on a 130-nm CMOS process. Fig. 7 shows the proposed amplifier’s layout and Table II resumes the amplifiers specs on 130-nm.

V. CONCLUSIONS

A comparison between three OTA topologies for low distortion requirements was presented. The analysis results on a design constraint maximizing the output swing in order to reduce non-linear behavior from transistors. However, if the preamplifier stage on a two stages scheme has more than three piled transistors, distortion levels become significant as is the case on folded cascade topologies. The proposed amplifier is to be used for an analog front-end for PSPMTs based gamma detectors for medical applications.

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