A Tunneling Model for Gate Oxide Failure in Deep Sub-Micron Technology

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Abstract

Parametric failures in CMOS IC nanoelectronics, leads to strong detection problem. In order to develop new defect oriented test methods, it is of prime importance to study the behavior of the transistor affected by those kind of failures. In this paper, we present a new electrical transistor model, which allows to study the impact of gate oxide thickness drop. It is shown that electrical behavior of the proposed model matches in a satisfactory way the defective transistor behavior.

1. Introduction

Aggressive scaling down in microelectronics to achieve higher performance and high circuit density leads to use thinner gate dielectric. The thickness could reach 1.5 nm, which represents only 6 atomic layers. The last step of the oxide degradation (breakdown) has been widely studied and numerous Gate Oxide Short (GOS) model have been proposed [1-4]. After a presentation of gate oxide thickness drop and their associated behaviors, we present a new electrical transistor model to study gate oxide thickness drop at circuit level. Then, some simulation results are shown for several oxide failure configurations.

2. The gate oxide drop

Figure 1 shows two kinds of failure which can appear within the gate oxide layer of an NMOS transistor with ultra-thin SiO2 layer. We call “uniform defect” a lack of one or two atomic layers distributed all over the gate oxide (cf. Fig. 1.b) and “localized defect” a surface defect where locally tox = 1.2 nm (cf. Fig. (1.c) and (1.d)). These non uniformities may have different origins such as the roughness of the oxide surface, a lithographic problem due to a mask damages or an over/under etching due to a recipe drift. When the oxide thickness decreases, gate leakage current increases as well as for NMOS or PMOS transistors. In literature, different examples of this phenomenon are given for PMOS considered as the worst case as example on Figure 2 [5].

3. Electrical Model

3.1. Transistor model with gate leakage current.

Firstly, to model the non uniform atomic layer drop of the transistor gate oxide, we have introduced the gate leakage current in a classical charge sheet model [6]. Figure 3 shows the schematic view of an elementary transistor with ultra thin gate oxide and gate leakage current, called GLNMOS.

Then a segmented model is used to study non uniformity only along the channel length and matrix model is used to study impacts of a random local defect.

3.2. Segmented Model and Matrix description

As presented Figure 4.a, to support channel current variation of a defective structure, the structure is cut into N juxtaposed GLNMOS. For given gate (VGS) and drain (VDS) voltages, the segmented model is used to resolve a system with N equations and N − 1 unknowns to determine the quasi-Fermi level, ΦC, at the GLNMOS boundaries to respect the law node at each node. To study the surface defect impact, we used a lumped-element
model [7] with GLNMOS transistors to compose the horizontal array (black color on Fig.4.b) and classical transistor without gate leakage current, to compose the vertical array (gray color on Fig.4.b).

Figures 6 shows the same electrical characteristics as Figure 5.a illustrates gate current \( I_G \) versus gate the segmented model for a non defective transistor. Figure 5 shows electrical simulations realized with a 10x10 network of elementary transistors (b).

4. Simulation results and Discussion

Figure 5 shows electrical simulations realized with the segmented model for a non defective transistor.

![Figure 4: Schematic view of segmented model with several GLNMOS (a) and Matrix model with a 5x5 network of elementary transistors (b)](image)

Figure 5.a illustrates gate current \( I_G \) versus gate polarization, \( V_{GS} \), which have similar behavior than the experimental density gate current characteristics plotted on Figure 2.b. This qualitative analysis allows to validate our model with regard to the characteristic behavior.

![Figure 5: Simulation of \( I_G \) versus \( V_{GS} \) characteristics (a) and \( I_G \) versus \( V_{GS} \) characteristics (b) for the reference transistor with \( t_{ox}=1.5nm \) and \( W\times L=10x10\mu m^2 \).](image)

Figure 5. Simulation of \( I_G \) versus \( V_{GS} \) characteristics (a) and \( V_{GS} \) versus \( V_{DS} \) characteristics (b) for the reference transistor with \( t_{ox}=1.5nm \) and \( W\times L=10x10\mu m^2 \).

Whatever the defect localization, the gate current \( I_G \) grows of 40% for \( V_{GS}=1.2V \) (cf. Figure 7). On Figures 8, we also observed this straight impact of the defect localization on the transistor channel \( \Phi_E \) behavior.

![Figure 8: Simulation of the quasi-Fermi level, \( \Phi_q(x,y) \) distribution for the reference transistor with \( t_{ox}=1.5nm \) (a) and for defective transistors with localized defect (b), and for \( V_{GS}=50mV \) and \( V_{DS}=1.2V \) (c).](image)

5. Conclusions

In this paper, we have presented a new electrical transistor model, which allows to study the impact of gate oxide thickness drop. Based on a classical charge sheet model approximations, we have developed a segmented model to investigate a uniform reduction of the oxide thickness. Then, we have created a matrix model to study gate oxide bi-dimensional defects. It has been shown that the behavior of the both models match in a satisfactory way the experimental measurement behaviors.

6. References