Abstract- A single-stage, ZVT-PWM, power factor correction converter is proposed in this paper. Zero-voltage switching for the main switch and zero-current switching for the auxiliary switch are realized by utilizing the leakage inductance of the output transformer and the capacitance of the switches. As a result, no additional resonant components need to be added. ZVS operation is realized for wide range of load and line. High frequency operation of the proposed converter makes the ac-dc power supply possible to be minimized in size and weight and the soft switching scheme will reduce the electromagnetic interference (EMI). The proposed converter uses a grounded auxiliary switch so that the isolated driving circuit is not required. The simplified driving circuitry again improves the overall efficiency and power density. Practically, the direct driving schemes of both the main and the auxiliary switches allows the proposed converter to operate in even high switching frequency and have good regulation capability. A 50-W 500-kHz prototype has been built in the laboratory to experimentally verify the analysis and simulation results.

Moreover, with the residential and defense industry continuously demanding for even higher power density, switching mode power supply operating at high-frequency to reduce size and weight of circuit components. But with the increasing of switch frequency, the switching loss becomes intolerable, resulting in very low conversion efficiency. Furthermore, the presence of leakage inductance in the high-frequency transformer and junction capacitance in the semiconductor devices causes the power devices to turn-OFF and turn-ON with more energy loss and noise. Because of this reason, the switching frequency of the traditional SMPS (Single Mode Power Supplies) is limited to 100kHz. To boost the switching frequency, various soft-switching techniques have been introduced to alleviate the switching losses [3,4].

In this paper, a single-stage, soft switching power factor correction circuit is proposed. The principle of operation and the soft switching condition are presented along with simulation and some experimental results for a 50W @ 500kHz prototype.

I. INTRODUCTION

The growing concern about harmonic pollution coupled with the new international standards, there is a real demand on a clean power supplies with a low ac line harmonic contents. Yet the use of power supplies continues to increase and more distorted mains current is drawn from the line, resulting in lower power factor and high total harmonic distortion. This distortion problem becomes more serious when the loads become highly non-linear. Power factor correction (PFC) is becoming more and more common in single-phase off-line switching-mode power supplies. Not only because low power factor limits the maximum available power drawn from mains, but also agency regulation requires that the harmonic current of the line current of mains-connected equipment remains below certain limits. For many years a great deal of effort has been made to develop efficient and cost-effective power factor correction schemes. As a branch of active PFC techniques, the single-stage technique receives particular attention because of its low cost implementation [1,2].

II. PROPOSED CONVERTER AND ITS OPERATION

The proposed soft-switching converter in Fig. 1 is based on the hard-switching single-stage PFC converter with two bulk capacitors proposed first in [2]. Besides achieving zero-voltage transition (ZVT) for the main switch, the circuit also using an extra winding on the transformer core as a snubber, L_{ap}, to lower the voltage and the current stresses of the auxiliary switch. The diode D_l is added to prevent circulating current through D_a. C_s and C_a present the parasitic capacitance of S and S_a, respectively. L_{k1} and L_{k2} are the leakage inductance of the primary side transformer L_{p1} and L_{p2}, respectively.

The main waveforms and the equivalent circuits for the modes of operation are shown in Figs. 2 and 3, respectively. The mode of operations are discussed as follows:

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Mode 1: $t_0 < t < t_1$

Initially, it is assumed that $S$ was OFF and $C_s$ has an initial voltage of $V_{Cso}$ that is greater than $V_{in,rms}$. In this discussion, the input voltage will be assumed to be constant and equal to the $rms$ value of the line voltage ($V_{in,rms}$). At $t=t_0$, the auxiliary switch $S_a$ is turned ON. $C_s$ and $L_{ak}$, $L_m$ form a resonant tank as shown in Fig. 3(a) along with $L_{k1}$, $L_{k2}$. The resonant in the auxiliary branch will be the dominant on the soft switching condition; other branches will have a small reflected effect due to the transformer turns ratio. The voltage across the capacitor $C_a$ will drop to $V_{in,rms}$ at $(t=t_1)$. The key equations for this mode can be expressed as follows:

\[
v_{cs}(t) = \left(\frac{2n_i^n}{K_i(2n_i + n)} + n_i^n\right) \left[1 - \cos(\omega_0 (t - t_0))\right] + V_{Cso} \cos(\omega_0 (t - t_0))
\]

\[
i_{L_{ak}}(t) = \left(\frac{2n_i^n}{K_i(2n_i + n)} + n_i^n\right) \left[\frac{\omega_0 (t - t_0)}{Z_o} - \frac{\sin(\omega_0 (t - t_0))}{Z_o}\right] + \frac{V_{Cso} \sin(\omega_0 (t - t_0))}{Z_o} \left(\frac{n V}{Z_o}\right) \omega_0 (t - t_0)
\]

\[i_{Li} (t) = 0 \quad ; \quad i_{Do} (t) = 0 \quad \text{(Very small)}
\]

where,

\[n = \frac{n_i}{n_2} \quad ; \quad n_o = \frac{n_1}{n_2} \quad ; \quad \omega_o = \sqrt{\left(\frac{2n_i}{n_2} + 1\right)\frac{L_{ak}}{C_i} + K_L L_{ak}} ; \quad K_L = \frac{L_{ak}}{L_{li}} ;
\]

\[Z_o = \sqrt{\left(\frac{(2n_i/n_2) + 1)L_{ak}}{C_i}\right)} = \omega_o L_{ak}.
\]

Mode 2: $t_1 < t < t_2$

This mode starts when $\rho_{C} < V_{in,rms}$. The diode $D_i$ starts conducting a small current that will charge $L_i$. The effect of this mode on the resonant condition is very small and it has negligible effect on $L_i$, too, so that the equations from mode 1 will be valid during this mode except for $i_{Li}$ that will be very small ($i_{Li}(t) = 0$). At the end of this mode $(t=t_2)$, the capacitor voltage of the main switch $S$ reaches zero, allowing $S$ to be turned ON at ZVS during any time in mode 3. The time interval for this mode is given by:

\[
\Delta t_2 = t_2 - t_0
\]

\[
\alpha = \omega_o \Delta t_2 = \cos^{-1} \left(\frac{1}{1 - \frac{V_{Cso}(2 + (n/n_o))}{2Mn_o} + \frac{n}{2n_o} + 1}\right)
\]

where,

\[
V_{Cso} = \frac{V_{Cso}}{V_{in,rms}} ; \quad M = \frac{V_o}{V_{in,rms}}.
\]

Mode 3: $t_2 < t < t_3$

This mode will start after $V_{Cso}$ reaches zero and $D_S$ will carry the capacitor current and $L_i$ will start effectively
charging through the input voltage. \( I_{ak} \) will start linearly discharging. This mode will last until the \( I_{Ds} \) reaches zero. We can turn ON the main switch \( S \), at any time during this mode preferably at the end of this mode. A second resonant condition will occur if \( S \) is kept OFF that will result in raising the voltage across \( C_s \) and ZVT will be lost. Equations for this mode are given as follows:

\[
i_{lak}(t) = -\frac{n_o V_o}{L_{ak}}(t - t_2) + i_{lak}(t_2)
\]

\[
i_{ld}(t) = \frac{V_{in, rms}}{L_i}(t - t_2)
\]

\[
i_{lp}(t) = \frac{n_o^2 V_o}{n} \left[ 1 + \frac{1}{L_{ak}} \right] (t - t_2) - \frac{n_o i_{lak}}{n}(t_2)
\]

\[
i_{d}(t) = i_{lak} - 2i_{lp} - i_{li}
\]

The time interval of this mode is given by:

\[
\Delta t_3 = t_3 - t_2 = \frac{I_{slak} \cdot \left(1 + \frac{2n_s}{n}\right)}{n_o M \left[1 + \frac{2n_s}{nK_{l}} + \frac{2n_s}{n}\right] + \frac{1}{K_{la}}}
\]

where,

\[
I_{slak} = \frac{Z_i I_{lak}(t_3)}{V_{in, rms}}; K_{la} = \frac{L_a}{L_{ak}}
\]

Mode 4: \( t_3 < t < t_4 \)

After turning \( S \) ON at \( t=t_3 \), the choke current continues to charge up linearly. This period ends when the leakage inductor current \( i_{lak} \) reaches zero and \( D_L \) reverse biased. We can turn OFF the auxiliary switch \( S_a \) at any time after this mode With ZCS. The equations for \( i_{lak}, i_{li} \) and \( i_{lD} \) from mode 3 will be valid throughout this mode. The time interval is given by:

\[
\Delta t_4 = t_4 - t_3 = \omega_o \Delta t_4 = \frac{I_{slak} \cdot \left(1 + \frac{2n_s}{n}\right)}{n_o M} - \beta
\]

Mode 5: \( t_4 < t < t_5 \)

After turning \( S_a \) OFF at \( t=t_4 \), the inductors \( L_{k1}, L_{k2} \) will start charging through the stored energy capacitors \( C_{p1}, C_{p2} \), respectively. \( D_L \) will prevent the negative current in \( L_{op} \) and output current will increase linearly. This mode ends when the main switch, \( S \), is turned OFF at \( t=t_5 \). The equations in this mode are given as follows:

\[
i_{lak1} = i_{lak2} = i_{lak} = \frac{V_{cp} - nV_o}{L_e} (t - t_4)
\]

\[
i_{D_o} = 2n_i_{lak}
\]

\[
i_{lD}(t) = \frac{V_{in, rms}}{L_i} (t - t_4) + i_{lD}(t_4)
\]

The time interval is given by:

\[
\Delta t_5 = t_5 - t_4 = DT_s - \Delta t_4 = \phi = \omega_o \Delta t_5 = \frac{2\pi}{f_m} - \gamma
\]

where,

\[
f_m = \frac{f}{f_s}; \text{ and } V_{cp} \text{ is the average stored voltage in the capacitors } C_{p1} \text{ and } C_{p2}.
\]

Mode 6: \( t_5 < t < t_6 \)

At \( t=t_5 \), \( S \) is turned OFF. The main switch output capacitor \( C_s \) is quickly charged up by the current \( i_{lD} \) to the maximum value, \( 2V_{cp} \). Under the constraint of KCL, both the storage capacitors, \( C_{p1} \) and \( C_{p2} \) are being charged by the current \( i_{lD} + i_{lp1} + i_{lp2} \) during this operation period. With the inductor current \( i_{li} \) decreasing linearly, magnetic energy stored in the choke is being converted into electric energy and being stored into the storage capacitors. Thus the energy loss of the storage capacitors during the previous Mode is being recovered. Because \( L_{p1} \) and \( L_{p2} \) are relatively small, the duration of this mode can be neglected (\( t_o=t_6-t_5=0 \)).

\[
i_{lD}(t_o) = i_{D0}(t_6) = 0
\]

\[
v_{Cp}(t_o) = 2V_{cp}
\]

\[
i_{li}(t_6) = \frac{V_{in, rms}}{L_i} (DT_s + \Delta t_5 - \Delta t_2)
\]

Mode 7: \( t_6 < t < t_7 \)

The choke inductor current, \( I_{li} \), continues to decrease linearly. Owing to the existence of diode \( D_o \), the primaries of the transformer present very high impedance with the currents through the windings can be negligible. This period ends when the choke inductor current reaches zero.
the duration of this mode is given by:

\[ \Delta t_7 = t_7 - t_6 = \frac{i_{iL}(t_6)L_s}{2V_{Cp} - V_{in,nu}} \]

\[ \psi = \omega_c \Delta t_7 = M \left[ D \left( 2\pi f_w \right) + \gamma \right] / 2M - M_1 \]  

where,

\[ M_1 = \frac{V_o}{V_{CP}} \]

Mode 8: \( t_5 < t < t_0 + T_1 \)

This is a freewheeling stage used for regulation purposes. During this mode the voltage across the capacitor \( C_s \) reduced from \( 2V_{Cp} \) to \( V_{Cas} \). \( C_s \) enters a pre-resonant stage with \( L_{k1} \) and \( L_{k2} \).

\[ v_{Cp}(t) = V_{op} \left[ 1 + \cos((t - t_1) \sqrt{2/(C_sL_s)}) \right] \]
III. SOFT-SWITCHING CONDITION AND DESIGN EQUATIONS

A. Soft-Switching Condition

Soft-switching is maintained for this circuit if the main switch \( S \) turned ON during mode 3, interval \( \beta \), as explained in the circuit operation where:

\[
t_2 - t_o \leq t \leq t_3 - t_o
\]

B. Design Equations

From the study-state analysis above by controlling the time intervals we can achieve a specific design. In addition to Eqs. (1)-(5), the following equations can be derived to describe the converter operation:

1) Expression for the voltage gain, \( M \):

Using average input inductor current that be obtained from the conservation of power principle in lossless circuit as expressed in the following relation:

\[
I_{\text{ave}} = I_s V_o
\]

\[
\frac{V_o}{V_{\text{in}}} = M = \frac{I_{\text{ave}}}{I_o} = \frac{I_{L\text{ave}} R_o}{V_o}
\]

It can be shown that once an expression for the average input current is obtained, the voltage gain may be given by,

\[
M = D_2 + (\beta f_s^2/4\pi^2) + (D\beta f_{\text{ave}}/\pi) \left[ 1 + \frac{M_1}{2M - M_1} \right]
\]

where, \( \tau \) is the load time constant given by,

\[
\tau = \frac{L}{R}
\]

and the normalized load time constant is given by,

\[
\tau_n = \frac{\tau}{I_o}
\]

2) Average output diode current:

The average output current is given by,

\[
i_{\text{ave}} = \frac{V_o}{R_o} = \frac{1}{T_o} \int_{t_o}^{t_2} i_{\text{in}}(t) \, dt
\]

Solving for \( \tau \) we will have,

\[
\tau_n = \frac{n\phi^2 f_s^2 K_{\text{LL}}}{4\pi^2} \left[ \frac{1}{M_1} - n \right]
\]

where, \( K_{\text{LL}} \) is an inductor ration.

3) Resonant inductor current at \( t = t_2 \):

Using \( i_{\text{Lak}}(t) \) from Mode 1, we obtain

\[
i_{\text{Lak}}(t_2) = \left( \frac{2n^2 V_o}{K_k(2n_o + n)} \right) \left[ \frac{\alpha \sin(\alpha)}{Z_o} - \frac{n_o V_o}{Z_o} \right] + V_{\text{con}} \sin(\alpha) \]

than the normalized current is,

\[
i_{\text{Lak}} = \left( \frac{2n^2 M}{K_k(2n_o + n)} \right) (\alpha - \sin(\alpha)) + V_{\text{con}} \sin(\alpha) - n_o M \alpha
\]

where,

\[
V_{\text{con}} = \frac{V_{\text{con}}}{V_{\text{in}}}
\]

4) Initial voltage on the resonant capacitor:

Using \( v_{\text{Lal}}(t) \) from Mode 8 to yield the following expression:

\[
v_{\text{Lal}} = v_o(t_o + T_o) = v_0 \left[ 1 + \cos(\Delta t_o \sqrt{\frac{2}{C_o L_o}}) \right]
\]

where,

\[
\Delta t_8 = t_o + T_o - t_1
\]

and by defining,
\[ \rho = \omega_o \Delta t_b, \]

the above equation becomes,

\[ V_{acv} = \frac{M}{M_1} \left[ 1 + \cos \left( \rho \left( \frac{2K_{L_d}}{K_{L_a}((2n_o/\eta) + 1)} \right) \right) \right] \quad (9) \]

5) Switching period:

By noting that the sum of time durations for all the modes is equal to \( T_s \), we have the following relation,

\[ \frac{2\pi}{f_{ns}} = \alpha + \beta + \gamma + \phi + \psi + \rho \quad (10) \]

6) Duty Cycle:

The expression for \( D \) is given by,

\[ DT_s = \Delta t_4 + \Delta s \]

Rewriting the equation using the normalized intervals we have,

\[ 2\pi \frac{D}{f_{ns}} = \gamma + \phi \quad (11) \]

The normalized parameters used in Eqs. (1)-(11) are the key for the converter design. Solving these equations numerically using MathCad, set of design curves of \( M \) vs. \( D \) under different normalized load values are obtained as shown in Fig. 4.

C. Design Example

Let us consider the following design specifications:

\( V_{in,\text{rms}} = 110V, \quad V_o = 28V, \quad P_o = 50W \) and \( f_s = 500kHz \). Using Fig. 4 for the following fixed circuit parameters,

\( f_{ns} = 0.053, \quad K_{L_d} = K_{L_a} = 11.7, \quad K_L = 166, \quad n = n_o = 2.667, \)

we can obtain the following converter design parameters.

\( M = V_o / V_{in,\text{rms}} = 0.255, \quad I_o = P_o / V_o = 1.786A, \)

\( R = V_o / I_o = 15.68\Omega, \quad \omega_o = 2\pi f_s / f_{ns} = 59.76\text{Mrad/sec}. \)

For a given \( M = 0.25 \) and \( \tau_n = 1.1 \), the estimated duty cycle is \( D = 0.23 \). Based on these values, the converter circuit components are:

\[ L_i = \tau_n R / f_s = 35\mu\text{H}, \quad L_{ak} = L_{k1} = L_{k2} = L_i / K_{La} = 3\mu\text{H} \] and \( C_i = \frac{(2n_o / n) + 1}{L_o \omega_o^2} = 280\text{pF} \)

![Fig. 5: Simulation Schematics](image_url)

![Fig. 6: Simulation Results](image_url)

IV. COMPUTER SIMULATION AND EXPERIMENT RESULTS

Using the component values from the above design example, Pspice circuit shown in Fig 5 is simulated to produce the result shown in Fig 6. And to verify the steady
state operation of the proposed converter shown in Fig. 1, a 110V/60Hz input, 28V/3.5A output experimental prototype was built. The following key components were used in the implementation of the experimental circuit: Input inductor \( L_i = 35\mu H, 3F3 RM10 \) core; Transformer — Philips 3F3 RM12 core, \( N_{p1} = N_{p2} = N_{a1} = 16T, L_{ak}=L_{a1}=3\mu H \); Switches — \( S: \) IXFH20N60; \( S_a: \) IXTP3N90A; Storage Capacitors — 220\( \mu F/250V \); Diodes — \( D_i, D_{L}, D_p: \) DSEI 1210A; Low voltage rectifier diode \( D_0 — 3CPQ060 \); Switching frequency — 500kHz. Fig. 7 gives the measured line voltage and current waveforms, resulting in power factor of 0.987. In Fig. 8, the voltage across the main switch and its drain current are shown. As shown, just before \( S \) is turned \( ON \), its body diode carries the reverse current, hence, achieved zero-voltage turn \( ON \). Finally, Fig. 9 shows the auxiliary switch, \( S_a \), current and voltage. From Fig. 8 we can estimate \( \Delta t_2 = 50\text{msec} \), from the theoretical calculation \( \Delta t_2 = 55\text{nsec} \) and the simulation gives about 65nsec which are in a good agreement.

VI. CONCLUSION

Due to high frequency operation, the proposed converter makes the design of unity power factor ac-dc power supply possible with high power density. At the same time, the active single-stage PFC techniques help to reduce the component count and cost and by utilizing the leakage inductance of the output transformer and the capacitance of the switches, so that no additional resonant components are need. Moreover, the proposed converter operates in DCM, using simple controller design with grounded auxiliary switch so that the isolated driving circuit is not required. The proposed converter could be considered as a strong competitor in low power application.

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