ABSTRACT

A new method for estimating the glitching contribution to the power dissipation of multilevel combinational logic circuits based on complex-time cellular automata is presented for the first time. To bridge the gap between continuous time, in which the combinational logic circuits operate, and the discrete time, in which cellular automata operate, the concept of complex time is introduced. Both the logic combinational circuit and the cellular automaton model that simulates it, are assumed to exist in a linear complex space, where the real part of the complex time is the continuous time and the imaginary part is the discrete time. Using the complex time concept the proposed model can take full advantage of both the powerful local operation capabilities of cellular automata, and the convenient formulation of VLSI circuit description using two-dimensional matrices and netlists.

1. INTRODUCTION

Power dissipation is recognized as a critical parameter in modern VLSI design field. The development of competitive market sectors such as wireless applications, laptops, and portable medical devices, depends on the power consumption as the most important parameter because the growth rate of the battery technologies is not so promising. Additionally, issues such as electromigration, reliability, chip overheating and packing selection are strongly dependent on the power dissipation. In recent years, efficient low power design techniques and power estimation methodologies have been developed to solve certain issues at all design levels [Rab96, Cha92, Sin95].

A large number of power estimation methods for combinational logic circuits have been reported in [Nai95]. Accurate estimation of power dissipation is a significant task needed to assist design and synthesis tools in their attempt towards designing low power circuits. Power dissipation in a CMOS circuit is directly related to extent of switching activity of the nodes in the circuit. In [Ben94] it was shown that hazard contribution to power dissipation in CMOS ICs (glitch power) cannot be neglected. A number of research approaches for reducing the power dissipation coming from glitching activity were proposed [Dev92, Now95, Lin95]. The use of symbolic simulation in order to produce a set of Boolean functions representing conditions for switching at each gate in the circuit has been proposed in [Dev92]. Nowick et al [Now95] has developed an exact two-level minimizer that combines a number of existing ideas on this problem. In [Lin95] a method for synthesizing a hazard-free multilevel logic implementation from a given implementation. The method is based on Binary Decision Diagrams and is applicable to multiple-output logic functions.

Fig. 1: All the events that take place in real time between two successive time steps in imaginary time, \( t_i^n \) and \( t_i^{n+1} \), are mapped to \( t_i^{n+1} \) in the discrete time.

The method for the estimation of glitching power of multilevel combinational circuits presented here is based on complex-time cellular automata (CAs). CAs have been extensively used among others as a VLSI architecture [Pri86, Tsa92], as pattern generators for VLSI testing [Das93, Kar98], and in ASICS for image processing [Kar96, And96, Kar97]. The combinational logic circuits operate in continuous time, whereas CAs operate in discrete time (i.e. the states of all cells are updated simultaneously at discrete time steps). To bridge the gap between the continuous time (logic circuit time) and the discrete time (cellular automaton model time), the concept of complex time is introduced. The \{circuit-model\} system is assumed to
exist in a linear complex space, where the real part of the complex time is the continuous time and the imaginary part is the discrete time. Using the complex time concept the proposed model can take full advantage of both the powerful local operation capabilities of CAs, and the convenient formulation of VLSI circuit description using two-dimensional matrices and netlists. Furthermore, the introduction of complex time may allow the use of sophisticated mathematical tools, such as conformal mapping [Soc76] for the determination of power dissipation in combinational logic circuits.

2. DESCRIPTION OF THE METHOD

A combinational logic circuit with n elements (nodes) and m nets is represented by a graph \( G(Q, E) \), where \( Q=\{q_j \mid j = 1, 2, 3, ..., n\} \) is the element (node) set and \( E=\{e_j \mid j = 1, 2, 3, ..., m\} \) is the net (edge) set. The connectivity of the circuit is described by the connectivity matrix \( M \), the elements of which are given by [Sai95]:

\[
m_{jk} = \begin{cases} 
1, & \text{if element } j \text{ is connected to element } k \\
0, & \text{if element } j \text{ is not connected to element } k 
\end{cases}
\]

(1)

The netlist of the circuit is given the same way as in any VLSI circuit [Sai95].

To estimate the power dissipation in glitches the circuit is also represented by a cellular automaton (CA) by considering each circuit element as a CA cell. The CA is two-dimensional and has not the regular matrix-like topography. The circuit connectivity matrix \( M \) gives the connections between CA cells. Both the logic combinational circuit and the cellular automaton model that simulates it, are assumed to exist in a linear complex space which is spanned by \( \{V, t\} \). \( V \) is the complex voltage given by:

\[
V = V_r + iV_i
\]

(2)

\( V_r \) and \( V_i \) are the real and imaginary parts of the voltage, respectively, and \( i^2 = -1 \). Since there is no use for the imaginary part of the voltage, it is taken to be equal to zero. The following relations hold:

\[
V_i = 0 \\
V_{ss} \leq V_r \leq V_{dd}
\]

(3)

where \( V_{ss} \) and \( V_{dd} \) are the ground and power voltages, respectively.

Complex time \( t \) is given by:

\[
t = t_r + it_i
\]

(4)

t_r and \( t_i \) are the real and imaginary parts of the time, respectively. The real part of the time \( t_r \) represents the time in which the circuit operates, whereas the imaginary part \( t_i \) is the discrete time in which the CA operates.

3. APPLICATION OF THE METHOD

The method described in the previous section is applied to three simple circuits shown in Figures 2, 3, and 4. The gate delays have been obtained from the

![Fig. 2: (a) A logic circuit, and (b) the input-output waveforms obtained using the proposed method in the case of synchronized (up) and unsynchronized (down) inputs.](image-url)
technology files of a 0.7 μm process. Figure 2(a) shows a logic circuit. The input-output waveforms obtained using the proposed method in the case of synchronized and unsynchronized inputs are shown in Figure 2(b). Figures 3(a) and 4(a) show logic combinational circuits and Figures 3(b) and 4(b) show the input-output waveforms obtained using the proposed method. In all cases the glitching in the waveforms has been successfully obtained and the estimation of power dissipation is straightforward.

Fig. 3: (a) A logic circuit, and (b) the input-output waveforms obtained using the proposed method.

4. CONCLUSIONS

A new method for the estimation of glitching power in combinational logic circuits based on complex-time cellular automata is presented for the first time. To bridge the gap between the continuous time, in which the combinational logic circuits operate, and the discrete time in which cellular automata operate, the concept of complex time is introduced. Both the logic combinational circuit and the cellular automaton model that simulates it, are assumed to exist in a linear complex space, where the real part of the complex time is the continuous time and the imaginary part is the discrete time. Using the complex time concept the proposed model can take full advantage of both the powerful local operation capabilities of cellular automata, and the convenient formulation of VLSI circuit description using two-dimensional matrices and netlists. Using this model we introduced continuous and discrete time in Boolean functions, in the solid mathematical framework of linear complex spaces. The introduction of complex time may also allow the use of sophisticated mathematical tools, such as conformal mapping, for the determination of power dissipation in combinational logic circuits.

Fig. 4: (a) A logic circuit, and (b) the input-output waveforms obtained using the proposed method

5. REFERENCES

Minimization of Hazard-Free Logic with Multiple-
Input changes,» IEEE Trans. on Computer-Aided

[Dev92] S. Devadas, K. Keutzer, and J. White,
«Estimation of Power Dissipation in CMOS
Combinational Circuits Using Boolean Function
Manipulation,» IEEE Trans. on Computer-Aided

[Pri86] W. Pries, A. Thanailakis, and H. C. Card,
«Group properties of cellular automata and VLSI
applications», IEEE Transactions on Computers,

[Tsa92] Ph. Tsalides, A. Thanailakis, N. Pitsanis, and
G.L. Bleris, «Two-Dimensional cellular automata:
Properties of a new VLSI architecture» The

theoretic analysis of additive cellular automata and
its application for pseudoehaustive test pattern
generation» IEEE Transactions on Computers,

[Kar98] I. Karafyllidis, I. Andreadis, Ph. Tsalides,
and A. Thanailakis, " Non-linear Hybrid Cellular
Automata as Pseudorandom Pattern Generators for
VLSI Systems." VLSI Design, vol. 7, pp. 177-
190, 1998.

Tsalides and A. Thanailakis, "A Cellular
Automaton for the Determination of the Mean
Velocity of Moving Objects and its VLSI
Implementation", Pattern Recognition, vol. 29, no.
4, pp. 689-699, 1996.

[And96] I. Andreadis, I. Karafyllidis, P. Tzonas, A.
Thanailakis and Ph. Tsalides, "A New Hardware
Module for Automated Visual Inspection Based on
a Cellular Automaton Architecture", Journal of
Intelligent and Robotic Systems, vol 16, pp. 89-102
1996.

[Kar97] I. Karafyllidis, A. Ioannidis, A. Thanailakis
and Ph. Tsalides, "Geometrical Shape Recognition
using a Cellular Automaton Architecture and its
VLSI Implementation", Real-Time Imaging, vol. 3,

[Soc76] I. S. Sokolnikoff, and R. M. Redheffer,