Non-contact Testing for SoC and RCP (SiPs) at Advanced Nodes

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Abstract

Non-contact methods for testing System-on-Chip (SoC) and System In Package (SIP) assemblies are presented. This method allows for high speed testing at the wafer level for SoCs as well as testing during and after assembly for panel or wafer level SIP technologies. Wafer testing at advanced nodes is carried out without damaging underlying metallurgy - an issue with current contact testing techniques. The technology utilizes non-contact GHz short-range transceivers to transfer test signals and results to and from SoC ICs. The wireless probes convert standard tester ATE logic levels to high frequency RF (GHz) transceiver signals and thus allow the use of standard test equipment. A reduced set of contact probes are used for test power only. A 45 nm fully CMOS compatible IC with wireless test transceivers is designed and fabricated. Enhancing the reliability and economics of IC manufacture by enabling non-contact testing of SoCs before and during packaging is a key benefit of this technology.

1. Introduction

The relentless drive to produce cheaper and better consumer and industrial products has compelled the Semiconductor Industry to continue to innovate. Semiconductor manufacturers continue to shrink designs to gain more functionality per unit IC area. Innovations such as new conductors and new insulators have enabled devices to follow the 90nm, 65 nm, and now 45 nm feature size, ‘technology node’ trend [1]. These innovations have not been without engineering challenges. They also create technical challenges in terms of packaging and testing the resultant devices.

Advanced nodes enable the design of System(s) on Chip (SoC), where a system is implemented on a single die. With 100s of millions of transistors it is possible to create an almost complete system which may include memory, multiple processing units and signal conditioning, etc. To achieve the increased density and small feature size, materials science has played a key role.

One property of these new materials, specifically the ultra low-k (ULK) dielectrics used in advanced nodes, is increased mechanical compliance. The compliance of these ‘softer’ materials is greater than that of earlier generations of ‘hard’ dielectric materials. Fig 1 shows experimental data highlighting the large compliance of a 45nm ULK based bond pad compared to standard Silicon IC bond pad. This figure shows that an ULK dielectric needs only a fraction of the force, to cause the same mechanical deformation as traditional ‘hard’ dielectrics. The data was obtained using a Hysitron TribolIndenter on the types of ICs shown in Fig 7 (ULK 45nm) and Fig 10 (traditional Si 130nm). This compliance can cause mechanical damage to adjacent and underlying structures - including layers of conductors, if the ICs are subject to mechanical processing for packaging [2] or probing [3] for testing. This damage leads to broken connections in the thin metallization layers used in these ICs. Thus, while the advance of ever shrinking and denser devices is achievable, there is a cost in manufacturability, yield, test and ultimately, device reliability.

Figure 1 Ultra low K dielectric and standard Silicon IC bond pad compliance.

The Semiconductor Industry Association (SIA), 2006 [4], in fact, reports that the ‘Difficult Challenge’ category includes:

- Non-contact Testing for SoC and RCP (SiPs) at Advanced Nodes

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'Test for yield learning critically essential for fab process and device learning for below optical device dimensions'.

And;

'Potential yield losses due to mechanical damage during the testing process'.

**SoC testing issues:**

- Compliant ultra low k dielectric.
- Probing forces damaging circuits adjacent or underneath (circuit under pad).
- Delamination of dielectric at 45 nm.
- Decreased Die Pad Pitch – mechanical probe limits set an artificial boundary on die pad density or pitch, which can lead to a proportional impact on the device die size.
- Pressure required to get good contact may deform a large area with unknown circuit consequences.
- Wafer scale contact testing requires precision placement and large mechanical forces on prober, probe card, and wafer chuck.
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- Wafer scale contact testing requires precision placement and large mechanical forces on prober, probe card, and wafer chuck.

Following the trend of ICs before them, the cost of testing an SoC can increase more rapidly than its manufacturing cost; especially since SoCs are inherently more complex than previous generations of designs. An SoC has the functional complexity of a number of discrete ICs, compounding the testing issues with the inability to provide test access or test points for the growing number of internal signals which are not brought out to pads. Rapid growth in the highly cost-conscious consumer and communications applications has driven the need for SoC designs. Some mitigation of the testing issues are being implemented with Built in Self Test (BIST) [5] [6] and Design for Test (DFT) [7] approaches. Nevertheless the fragility of SoCs is a problem that needs to be addressed.

While SoCs have evolved to be very complex, they typically still need to be coupled to other elements to create a true system. Passives and incompatible elements like power amplifiers are being combined into systems by means of various advanced packaging techniques.

The SIA defines a System in Package (SiP) as any combination of semiconductors, passives, and interconnects integrated into a single package [8]. Like the testing challenges of SoCs, the testing of such heterogeneous SiPs is a significant and growing problem in the electronics manufacturing industry, where current test technology allows testing only after complete assembly and packaging of the SiP.

SiPs are analogous to PCBs in the sense that multiple chips and passives are combined onto a common substrate. SiPs may use passive components and dies of various technologies, (e.g. Si, SiGe, .13um, .25um, digital, analogue, RF, bare die, flip chip ICs etc.) integrated into a miniaturized package solution.

**Figure 2 SiP Market Projection (Source: Dataquest, 2006)**

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And;

‘Potential yield losses due to mechanical damage during the testing process’.

**Figure 3 i275 GSM EDGE radio-in-package using Redistributed Chip Package (RCP) (courtesy Freescale Semiconductor).**

Unlike PCBs, the miniature size of SiPs requires sometime unique and often expensive test solutions. This is predominately driven by high level of functional integration that requires additional tester instrumentation and costly test hardware. Rapid growth in the highly cost conscious consumer electronics and communications industries has increased demand for SiP and therefore SoC solutions (see Fig 2). One of the more cost sensitive applications in these industries has been the converged mobile devices such as the Smartphone.

SIP approaches include traditional, IBM; Multi-Chip-Module (MCM) [9], NXP; Passive Integration Connecting Substrate (PICS) [10] [11], and Freescale; Redistributed Chip Package (RCP) Freescale [12] [13] etc.
Radio-in-package (Fig 3) is an example of a SiP enabled by combining complex SoCs with heterogeneous ICs such as an RF power amplifier and transceiver as well as multiple passive components such as crystals, SAW filters, resistors, and capacitors. Some packaging technologies such as RCP are amenable to wafer scale (massively parallel) assembly techniques which offer highly economic volume production. The combination of SoC and especially wafer scale RCP is a powerful economic solution to the need for continued product economies.

SiP techniques require the use of Known Good Die (KGD) to be economically feasible. The fragility of advanced SoCs makes them even more prone to yield loss due to contact probing than earlier ICs. The KGD challenge is larger for advanced node SoCs because of this.

Each IC in a SiP solution can have a negative impact on yield and cost effectiveness. Therefore, the use of KGD in SiP is essential. Typically a SiP is not tested until after the package assembly process. In some cases, the intermediate testing is done during the assembly process but this leads to additional process complexity and cost.

Even with the ability to test devices as they are added to SiPs, it is atypical due to manufacturability concerns and hardware cost constraints.

At die level test, an issue shared between SiPs and ICs is that probe testing requires touchdown and scrubbing of IC pads. Scrubbing creates some damage on the die pads. This affects the ability to reliably “wire” the die using conventional interconnect technology such as wire bonding or more advanced techniques such as flip chip or RCP.

Repair and retest of wafer level SoCs is not viable for high volume consumer products given their cost constraints and assembly and construction methods.

2. Contactless Testing

2.1 SoC Wireless Testing

The ability to test SoCs in a contactless manner (Fig 4) would improve yield by reducing mechanical damage and enable more robust manufacturing during the package assembly process. It is well known that the die pad damage caused by the touchdown of contact probes used during die level test can impact follow-on manufacturing steps leading to lower yields, the need for re-test and resulting in higher product cost. This is particularly true for advanced nodes where the fragility of the compliant structures makes the cost to produce a known good die higher than previous generations of ICs. The cost of test is a complex issue where the measurement act itself can lead to higher costs in terms of yield loss and reduced processing ability for later steps.

The KGD can be compromised in terms of pad damage and creating particulate debris by contact probing. With advanced nodes a new complication of underlying structural damage by contact testing is an issue.

Another reason die level testing maybe limited for SoCs is that the number of signals/pads is typically large. Functional level testing of such devices can be cost prohibitive and physically impractical due to the Automated Test Equipment (ATE) configuration requirements, functional limitations, and test hardware complexity.

The authors have developed multi-scale wireless transceivers at the 130nm [14] and now 45 nm nodes to address the contact testing issue by providing wireless transceivers for medium and high-speed communications to SoCs.

Contactless testing beyond that may exist internal to an SoC is possible by the use of advanced scan techniques. I/O pads can be tested wirelessly, especially if the test interface can be operated at high speed using the scan technique described by Sunter, Muhtaroglu et al [15] [16].

Figure 4 SoC wireless test

In advanced nodes, power for IC test may be applied using conventional contact probe techniques and bus structures located in the scribe area. These power bus structures would be relatively immune to mechanical compliance issues and structural damage. I/O signal, functional test would then be performed using the contactless IP located in the I/O cell. It should be noted that the power bus capability is constrained to a level sufficient for device level testing. One advantage of the wireless test interfaces described herein is that the power used is much less that that used for driving normal I/Os by contact methods. Kuroda [17] has shown that wireless I/O can be made to use much less power than that of line driving wired I/O.

2.2 RCP Wireless Testing

RCP process flow includes the following steps as shown in Fig 5:

a) The dies are placed active side down on a substrate and encapsulated.

b) The substrate is removed.

c) Signal, power and ground are redistributed to connect SoCs with ICs and passive devices.
d) BGA solder balls are deposited (for package connections).
e) The panel or wafer is sawed into individual packages.

One potential major advantage of the RCP packaging method is that the chip to chip interconnects does not inherently require large pads. The fact that pad pitch can be made small enables smaller dies. Currently, contact probes limit the reduction of pad pitch and therefore can actually define the minimum die size and create what is known as “white space” in the die design. Obviously, this has a negative impact on the die cost.

Because SiPs are normally tested only after packaging a test coverage gap is created between the starting dies and the final packaged SiP. This gap, or “test blind zone” can lead to yield and cycle time issues, especially on large volume products.

Figure 5 RCP process flow.

A typical packaging product flow can have as much as a week’s worth of KGD going into a process before packaged test results are known. At the end user level, a week’s worth of product can cost millions if there is no feedback into the production process.

Due to this coverage gap, yield improvement and cost reduction are very challenging. In the conventional SiP flow, die yield loss, assembly cost, and test cost are captured and loaded against the good units found after final test. Without partial assembly testing there is no opportunity to cull defective devices early in the manufacturing value chain. Yield loss due to mounting dies or passives remains invisible without the ability to test during production.

In a manner similar to wireless SoC testing, the authors propose that wireless transceivers in the SoCs can be used for testing RCP devices (Fig. 6).

Important feedback during the production process [18] [19] can be gained in addition to the basic earlier tests. This feedback relays information regarding any global or local physical faults, and even circuit-level faults, providing the process engineer the ability to respond earlier. Earlier feedback can lead to improved yield and thus an improvement in the economics of SiP and SoC manufacturing. With partial-assembly-testing the system of parts can be tested as they are assembled in RCP processes.

Scaling is important from a test throughput point of view. Chip to chip communications on RCP can be in the form of very high speed serial signals as well as medium speed logic signals. The 45 nm test interface chip (Fig. 7) includes both high-speed as well as medium speed, carrier based transmitters, receivers, and signal processing electronics.

Figure 6 Non-contact Probe Card Test for RCP SoCs

Because of the compactness of the advanced nodes, logic for scan chain control was included with almost zero cost in chip real estate. Included in the design are circuits under antenna structures to provide even more compact test interfaces as well as antennae of various pitches for consideration of spacing optimization.

Note that the wireless test interface method can be used at several of the RCP manufacturing steps. This is because with the RCP method the important active elements and antennae are close to the surface throughout the manufacturing process. In addition, metallization is exposed through several of the process steps enabling contact for power. The contactless test method with RCP substrates hereby enabling increased test throughput.

During RCP type SiP assembly, IC power can be applied in a relatively innocuous way because of the robustness of the RCP interconnect metallurgy. The wireless testing can then be carried out to test the effectiveness of the assembly process including hidden nodes which are not connected or used in the RCP or final product. This enables a window for testing the known good dies within the RCP process. This allows for consideration of potential dropouts and diagnosis of failures within the manufacturing process.
The ability to test between KGD and final test is a key advantage of the wireless method.

Figure 7 Non-contact DUT (left), probe (right), antennae (top of figure) in 45 nm technology.

3. System Design

The design of the wireless 45 nm transceiver circuits requires optimizing trade-offs between several parameters and design criteria.

In this design, several considerations need to be addressed:

- Scaling of multiple antenna designs to emulate various pad pitches found in different applications and process nodes.
- Designing both medium speed and high speed wireless transceivers to span a range of testing applications.
- Minimizing on-chip real estate requirements for antennae and transceiver circuits.
- Sufficient RF coupling range to allow for probe, DUT, SoC or RCP misalignment and prober over-travel.
- Sufficient intelligence in DUT transceiver to allow the testing of bare (wafer level) SoCs.
- Compatibility with standard ATE equipment at the interface of the wireless probe.
- Utilizing a base-line 45 nm CMOS process (not specialized RF or analog) for cost and multi-source purposes.
- Ensuring that RF components are not high power and do not interfere with other chip operation.
- Ensuring that RF components are robust from a susceptibility point of view to enable communications within a digital environment for both SoC and RCP applications.

3.1 RF Design

Many microfabricated antenna designs have been, and continue to be, researched for various applications such as clocking [20] and data transfer [21]. These designs are generally intended for non-test applications and do not meet the cost, performance and data integrity requirements for applications such as SoC testing. The designs presented here create RF transceivers meeting the cost and performance goals of test. Specialized RF CMOS technologies and other technologies like SiGe are not used for the stated economic reasons.

Although many designs may be used for transmitting and receiving data wirelessly, many are not suitable in wafer testing applications since they require a large power budget, or utilize large amounts of silicon real estate on the DUT or probe. Additionally, the bit error rate for testing purposes must be extremely low. The non-contact probe card technology presented uses surface antenna structures and CMOS transceiver circuits on the probe and DUT.

3.2 Silicon Chip Characteristics

In this design a GHz RF Carrier is used. This is a high enough frequency to allow miniature antennas to be used and yet low enough frequency to be built in base-line logic CMOS. A carrier frequency of ~1.5 GHz was chosen as a reasonable target and successfully simulated in the VLSI CAD tools. The uncertainties of the fabrication and device characteristics at this advanced node make this only an estimate. To rationalize the processes and compare to other nodes test structures were included that were used on production nodes of 180 and 130nm. Table 1 shows the design goals at various nodes. For a discussion of CMOS scaling and RF see reference [22].

Table 1 design goals for various nodes

<table>
<thead>
<tr>
<th>Node</th>
<th>180 nm</th>
<th>130 nm</th>
<th>45 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Carrier</td>
<td>800 MHz</td>
<td>1.0 GHz</td>
<td>1.2 GHz</td>
</tr>
<tr>
<td>Test Osc.</td>
<td>45 MHz</td>
<td>100 MHz</td>
<td>150 MHz</td>
</tr>
</tbody>
</table>

The wireless transceiver electronics required on the DUT can have a negative impact on chip real estate if not carefully designed. However at 45 nm the size of the transceiver elements is small and the antennas are placed on top IC metal layers which may otherwise be unused. Referring to the hybrid wafer probe system shown in Fig. 4, 6, and 10 during testing, the DUT is brought into close proximity (less than 100 μm) with the matching antenna.
array on a non-contact probe card. ATE is connected to a conventional wafer probe test system. Data signals (I/O) and power from the tester are transferred through the probe card to the DUT via wireless data signals and wired (contact probe) power contacts.

In one case the data signals modulate/demodulate a high frequency carrier generated by transceiver circuits, providing a wireless bi-directional data link between the probe and the DUT. In the other case the data signals create a truncated RF carrier signal which is transmitted between probe and DUT or vice versa. In the case of the short pulse the data rate is higher than which can be carried by normal probe equipment.

![Figure 8 SMA connector and 100x100um Nano-probe](image)

**Figure 8 SMA connector and 100x100um Nano-probe**

In this case we have designed and interfaced custom high speed wireless probes to test the signals. Fig. 8 is an example of one of these ‘Nano-Probes’.

The prober PCB supplies power to the non-contact probe in the standard way through the ATE probe card interface. Power to the DUT is supplied through a minimal number of probe needles from the probe card. For RCP SoC power is supplied from the DUT or, alternatively, directly from probe needles from the probe card. The reverse is also possible; that is DUT power from RCP substrate. In either case, the idea is to minimize the number of actual probe needle locations. Reducing the number of probe contacts reduces the complexity of the probe card. It also reduces the mechanical forces on the SoC wafer; a critical issue given the compliant nature at advanced nodes. Having reduced probe needles also reduces the scrub debris created by contact probes. Note that in the case of an RCP none of the SoC ICs require direct probe needle contact, a key advantage.

A critical task of this work is the design and performance of the microfabricated antennae and transceiver circuits used in the IC. These transceiver components (DUT and probe) are designed on a composite IC (Fig.7). One side of the chip is designed to be the probe while the other acts as the DUT. Sub-dicing can be used to separate them further.

4. **Experimental Results**

4.1 **Wireless Transceiver Design, RF Simulations, and results**

A discussion of basic antenna design and CMOS RF modeling for wireless and chip-to-chip communications can be found in several references [17] [23] etc.

Theoretically, antennas scale over all sizes and wavelengths. That is, size is directly proportional to wavelength, therefore antenna length, inductance and capacitance scale with technology size. However microenvironment is important and as well (in communications systems) noise - whether external or self induced, limits the capacity to send intelligence. The close proximity communications used herein are no different and in fact are likely susceptible to other issues like materials inconstancy or micro-environment electronics effects which normally are not a concern of the designer of a communications system. Simulation tools are insufficient to model these effects at the current time so that experimentation is required. In the current chip several different antenna sizes and micro-environments were included to provide guidance to future designs.

Standard CMOS CAD simulation tools were used as well as a preliminary process design kit (PDK) for the 45nm node was made available from one of the foundries.

Other design factors include:

- Number of metal layers: 7 available, 7 used
- RF design frequencies: .6-1.2 GHz carrier
- Antenna sizes/pitch: 40um to 120um

Because of the uncertainties involved in this advanced node, production access from three foundries is being obtained. ICs of a process matrix lot from one foundry are being tested to correlate cross-process and cross wafer variations. At the time of writing ICs from only two foundry are available.
One area of particular attention is the susceptibility to noise in a test environment. The high carrier frequency versus the relatively modest data rate helps to mitigate noise. In the design, an on-chip guard ring is placed away from the antenna, and careful consideration of Chemical Mechanical Polishing (CMP) design rules (metal fill), plus an N-well barrier was placed around the transceiver in the layout. This was done to reduce the susceptibility to interference caused by noise and to reduce coupling to the rest of the circuit. The area occupied by the transceivers at 45 nm is smaller than that of previous nodes possibly localizing the noise even further.

An RF spectrum analyzer (HP 8563A) a data analyzer (Tektronix CSA907R/T) and a high speed scope (HP 83480A) are used for data and carrier characterizations.

Figure 9 shows experimental results using the above noted Nano-probe signal from the 45nm IC. One can see a clear RF signal in this carrier based transmitter. In this case, the carrier is set by an external dc control signal to set the on-chip VCO/Carrier frequency. In this figure the carrier is set to ~750MHz.

The experimental data showed that the 45nm VCO design was controllable over a wider range than the design goal as shown in the following table. This demonstrates the mixed signal capability of this advanced node.

| RF Carrier design goal: | 0.6 to 1.2 GHz |
| Experimental Results:   | 0.2 to 1.5 GHz |

Carrier modulation is an important aspect of the design and the following experimental data shows that the RF carrier in the 45nm design is fully capable of high speed turn-on and turn-off. Fig 11 shows the RF carrier being turned on and off by a logic signal (lower trace) in a high speed manner > 350MHz. Because the data rate is beyond that of a standard digital (logic) I/O cell an analog I/O contact pad was designed to provide the input control while the RF was detected using a flying Nano-coupler. Then figure shows an effective data rate of approximately 700 Mbaud, which is much higher than the design goal of 20Mbaud.

In contactless face-to-face testing (DUT to probe) high speed bit error rate testing was carried out at various data rates and at various DUT to Probe distances.

It was found that the 45nm designs performed at a much higher data rate, >100MBaud, than the design goal of 20Mbaud during BERT testing.
Node  Data Rate  Error Rate
45nm  100Mbaud  no errors in 10\(^{13}\) bits

This represents a 500% improvement over the previous 130nm designs [14] from a data rate point of view. The actual limit appears to be the digital I/O cell used, not the RF transceiver chain. Because of the increased data rate extended error statistics were easily obtained and showed that no errors occurred in 10\(^{13}\) bits transferred at the 100Mbaud rate with a 50um DUT/Probe separation.

### 4.3 Parallel Probe System Physical Design

Fig. 10 shows the arrangement for multiple (4) non-contact RF probes in the middle of a traditional probe card. This picture shows a Quad 130 nm wireless probe design. The probe card provides power and I/O access between ATE equipment and the non-contact probe. Standard probe needles, seen on the periphery of the non-contact probe card, provide power to the DUT. The non-contact probe shown consists of 3 elements: Probe transceiver ICs, Ceramic transition hybrid, and Probe PCB. All of these conform to an industry standard format probe card.

This type of probe card can be used to SoC or, alternatively, SIP and RCP assemblies. The migration to 45 nm DUTs is a simple matter for this system as the wireless probe does not have to be 45nm technology. The probe card can use whatever technology is convenient it simply needs to be compatible with respect to footprint, carrier frequency and data rate.

![Figure 12](image)

Figure 12  100um antenna alignment, simulation versus measurement at constant signal level, lateral X and vertical Z offsets.

### 4.4 Alignment Testing.

Fig. 12 shows signal strength (normalized) versus vertical and lateral probe to DUT antenna alignment offsets. The measurements were on a 100um Manhattan antenna while the simulations were carried out using Transmission Line Modeling (TLM) software. The +z direction is that of greater separation (height) between probe and DUT antennas. The x axis refers to horizontal offsets between the center of the DUT and probe antennae. Zero on the x axis is where DUT and probe antennas are aligned and corresponds to the greatest coupling.

Fig. 12 also shows the physical range of reception for good wireless data transfer integrity. Shown are both simulated (EM simulation) and measured signals. Within the curve bit error rates are very low (<10\(^{-12}\)); outside the error rates are high. This shows the required wireless probe location, for good data integrity, is approximately +/-50um in the lateral direction, and 0 to 50um in the z direction with a good safety margin. This is well within the tolerances of modern prober equipment. Earlier work showed that the signal strengths are somewhat scale invariant with respect to antenna size if dimensions are scaled with distances [14]. This work also showed that the microenvironment of the antennas play a major role in off wafer signal characteristics.

Because the data path is completely wireless, data integrity does not depend on touchdown success or contact integrity. Contact integrity commonly characterized as Contact Resistance (CRs) is a major issue which complicates contact probing in various test scenarios [24]. CRs varies with probe age, condition, current load, pad microstructure, and contact pressure [25]. Values for CRs are often in the range of 1-10 ohms which in a 50 ohm RF system provide a large, random and uncontrolled, variable during testing. Wireless transceivers overcome this issue by bypassing contact uncertainty with RF signaling. Power-contacts, for test, are relatively easily done. With SoC designs, it is usual to have redundant power and ground contacts or one could use scribe areas to provide a modest level of power for testing.

### 5. System Level Discussion

The data integrity is important for testing. Simulation results at the 45 nm node show that they are comparable to that of a wired link, i.e. very low error rates. Testing confirms these results in the presence of manufacturing process variations and real-world effects such as chip parasitics and noise.

The choice of the 45 nm CMOS as a technology platform has not been a limiting factor in the communications and thus can enable low cost use.

The large standoff distance, ~50 um, for (medium speed < 100 MBaud) carrier based communication is flexible enough to be used in a wide variety of manufacturing situations. The short pulse communications >500Mbaud has several uses and could be used for testing at speed interfaces and devices within a SoC or SIP, RCP systems. This leads to another advantage of providing a wireless test interface - the ability to reduce test time by increasing test I/O speed.
6. Further Work

A standardized non-contact interface for SoC testing of various designs could be implemented using the technique shown in this paper. Such an IP block could be implemented as a standard interface which would be added to all SoC designs to provide a consistent test access portal. Universal and standardized non-contact transceivers for test could benefit manufacturers of ICs because tester resources could be amortized over many different designs without having to customize the tester resources and components.

At advanced nodes transistor leakage is greater than at earlier nodes. This may show up as increased noise in the communications system. Future testing will endeavor to characterize this factor.

6.1 Scaling of Designs

The transceiver sizes presented are quite small and can be placed under pads, and in our case under antennas, for a more compact design. As the circuits are migrated to smaller process nodes (130, 90, 64, and now 45 nm), the transceivers continue to shrink, pitches decrease, and operating frequencies can increase, as shown in Table 2.

Parallel data paths are enabled by smaller antenna sizes leading to higher speed testing. One limit is the basic cutoff frequency (fT) of the chosen technology. For the current design, the fT of digital CMOS would appear to be adequate for wireless communications. For the present time it is not clear what limits or advantages further VLSI scaling will bring to the RF aspect of this technique other than perhaps higher and higher frequency operation.

Table 2. Scaling to smaller process nodes

<table>
<thead>
<tr>
<th>Process (nm)</th>
<th>fT (GHz)</th>
<th>Area Factor ~L²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Node L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>180</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>130</td>
<td>60</td>
<td>0.5</td>
</tr>
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<td>90</td>
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</tr>
<tr>
<td>65</td>
<td>150</td>
<td>0.13</td>
</tr>
<tr>
<td>45</td>
<td>200</td>
<td>0.07</td>
</tr>
</tbody>
</table>

The wireless test transceiver circuits can easily be included in SoC ICs as an IP block. Like DFT or BIST this technique can augment the ability to produce KGD and provide more complete test coverage.

6.2 Future Work

Because of the reduced pin count enabled by the wireless test interface (zero data probe pins used), and the small footprint large economies can be brought to test, improving throughput and reducing test time. The high speed nature of the wireless technique can enable functional testing of elements with SoCs or SIPS. This can enable sorting and binning of parts.

It is worthwhile to investigate techniques to allow even greater standoff distance between DUT and probe transceivers. This may enable wireless packaged IC testing using the same wireless techniques. In this case the technology can follow the chip through all stages of its manufacture right up to the final package.

7. Conclusions

We have extended wireless chip testing into new applications, SoC and SIP, RCP and to an advanced node, 45 nm.

We have shown that wireless test techniques can be implemented in the latest technology nodes without the impairments of classical contact testing. We have also shown that this technique can be used to test the ICs and assemblies into the subsequent packaging processes such as RCP.

The relaxed alignment and standoff requirements for this technique over that of contact forms of testing allow the insertion of testing during package build up of RCP assemblies. With contactless testing, the mechanical destruction and stress upon SoC ICs is lessened, enabling higher yield.

This technology can use standard ATE, and probing equipment. It can be used to allow selected testing during assembly of simple or complex SoC and SiP systems. The RF transceiver technology is shown to be robust and can be used with various geometries. It can be built to accommodate various speed requirements. Antennae and transceiver circuits are designed to address practical VLSI design and production issues, and permit non-contact testing of SoC ICs and SIP wafers using hybrid non-contact test probes and transceivers.

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9. References


