**Abstract** — Negative bias temperature instability (NBTI), which causes temporal performance degradation in digital circuits by affecting PMOS threshold voltage, has become the dominant circuit lifetime reliability factor. Design for lifetime reliability, especially for NBTI-induced circuit performance degradation, is emerging as one of the major design concerns. In this paper, an NBTI-aware dual \( V_{th} \) assignment is for the first time proposed to simultaneously reduce the circuit leakage current and ensure the circuit lifetime requirement. Our experimental results on ISCAS85 benchmark show that the NBTI-aware dual \( V_{th} \) assignment not only assigns more high \( V_{th} \) gates in the ISCAS85 circuits and leads to up to 14.88% (average 3.46%) further leakage saving under 5% circuit performance relaxation, but also brings different optimal high \( V_{th} \) (on average 11mV higher) without performance relaxation.

**Key words** — Dual \( V_{th} \) assignment, Leakage current, Negative bias temperature instability (NBTI).

**I. Introduction**

Circuit reliability is one of the major concerns in VLSI circuits and systems design. NBTI (Negative bias temperature instability), which has deleterious effect on the threshold voltage and the drive current of semiconductor devices, is emerging as a major lifetime degradation mechanism\(^1\). When PMOS devices in circuits are stressed under negative gate voltage \((i.e., V_{gs} = -V_{dd})\) at elevated temperature, a shift in threshold voltage due to NBTI occurs. For example, \( V_{th} \) shifts due to NBTI can be as much as 50mV at 90nm technology node\(^2\).

Recently, researchers studied the circuit-level performance degradation models for NBTI based on the device-level NBTI models. Paul et al.\(^3\) proposed an estimation method of circuit degradation due to NBTI in digital circuits using a DC stress NBTI model. Some analytical models that evaluate NBTI effect with multi-cycle AC stress were then proposed to help designers estimate the circuit performance degradation due to NBTI\(^4\)\(^-\)\(^6\). A recursion process was used to evaluate the NBTI effect\(^5\) considering the signal probabilities and activity factors of gates, while Vattikonda et al.’s predictive NBTI model\(^4\)\(^,\)\(^6\) describes the effect of various process and design parameters.

Based on these analytical circuit degradation models, a few researchers have investigated design techniques to mitigate the NBTI-induced performance degradation. Kumar et al.\(^7\) studied the impact of NBTI on the read stability of SRAM cells and proposed a simple bit flipping technique to recover the static noise margin of SRAM cells. Paul et al.\(^8\) presented an NBTI-aware sizing algorithm to ensure the reliability of nano-scale circuits.

On the other hand, with the development of the fabrication technology, leakage power dissipation has become comparable to switching power dissipation\(^9\). At the 90nm technology node, leakage power may be up to 42% of the total power\(^10\). Many circuit level leakage power reduction techniques have been proposed, such as transistor sizing, body bias, dual \( V_{DD} \), input vector control, sleep transistor insertion, transistor stacking, and dual \( V_{th} \) assignment. Among these, dual \( V_{th} \) assignment technique\(^11\)\(^-\)\(^13\) assigns higher threshold voltage to some of the gates in the non-critical paths, in order to reduce the leakage current, while maintains the circuit performance due to the low \( V_{th} \) gates in the critical paths.

However, the performance constraints for the previous dual \( V_{th} \) assignment did not take the performance degradation caused by the lifetime degradation mechanisms into account. As we noticed that, the leakage current and NBTI are both affected by the threshold voltage \( V_{th} \). Higher \( V_{th} \) leads to smaller leakage current and smaller \( V_{th} \) degradation due to NBTI\(^14\)\(^,\)\(^15\). Therefore, the optimization for the leakage power through dual \( V_{th} \) assignment should also follow the performance constraints that ensure the circuit lifetime requirement.

This paper presents a novel NBTI-aware dual \( V_{th} \) assignment for both leakage reduction and lifetime assurance, and distinguishes itself in the following aspects:

1. An NBTI-aware delay model for gates under different \( V_{th} \) is first introduced for our NBTI-aware circuit optimization. New performance constraints: the performance requirement at a certain time interval in the future, are used in our NBTI-aware dual \( V_{th} \) assignment technique. Further we present our heuristic algorithm which includes a pruning method to greatly reduce the problem size.

2. Our experimental results on ISCAS85 show that with 5% performance relaxation, the NBTI-aware dual \( V_{th} \) assignment leads to about on average 3.46% more leakage reduction. Furthermore, the NBTI-aware dual \( V_{th} \) assignment technique brings higher optimal high \( V_{th} \) for the same circuit and leads to on average 3.44% further leakage saving without performance relaxation. With the usage of high \( k \) dielectrics, \( V_{th} \) may increase faster and make NBTI more important when you decide where to insert a high \( V_{th} \) gate.

3. Finally, we compare the NBTI-induced \( V_{th} \) variation with random \( V_{th} \) variation and show that the NBTI effect will have the same effect in the probabilistic based optimization, because the NBTI-induced \( V_{th} \) degradation influences the mean value of \( V_{th} \).

**II. Motivation Example**

Fig.1 shows a motivation example for our research. The circuit has 3 different paths. Given a performance (delay) requirement...
Designers try to assign high $V_{th}$ to as many gates as possible, such that the leakage reduction is maximized while the delay requirement is still met. However, under the influence of NBTI, during the $V_{th}$ assignment, one must consider the delay degradation as time goes by, and make sure that any path delay during the specific product life time [0, $T_{life}$] is not larger than the performance requirement $D_{req}$.

Fig.1(a) shows a simple solution to take into account the delay degradation due to NBTI. Without changing the conventional dual $V_{th}$ assignment algorithm, one can simply tighten the performance constraint to include the aging effect. For example, by simply setting a new timing constraint $D_1$ ($D_1 = D_{req} - \Delta D$, in which $\Delta D$ is the maximum delay degradation) at design time, one can obtain a $V_{th}$ assignment as shown in Fig.1(a), with $D_{path_i} \leq D_1$ ($i = 1, 2, 3$) at design time.

However, such a simple solution ignores the fact that gates with lower $V_{th}$ tend to age faster, while gates with higher $V_{th}$ have a slower degradation\cite{4}. For example, in Fig.1(a), path 2 has 2 gates with high $V_{th}$, while path 1 has none, therefore, path 2 has a slow aging rate. Be aware of such a difference, one may be more aggressive to assign more gates on path 2 with high $V_{th}$ (Fig.1(b)), even make it slower than path 1 at design time (Fig.1(b), $D_2 > D_1$), as long as the path delay $D_{path_i}$ ($i = 1, 2, 3$) at the end of life time $T_{life}$ can still meet the timing constraint $D_{req}$. Such an approach can achieve extra leakage savings (Fig.1(b) has one extra high $V_{th}$ gate than Fig.1(a)).

In this paper, based on the fact that gates with lower $V_{th}$ tend to age faster, while gates with higher $V_{th}$ have a slower degradation\cite{4}, and the leakage and delay degradation model (Section III), we develop a new dual $V_{th}$ assignment algorithm (Section IV), which uses a new timing constraint (i.e., $D_{path_i}$) at the end of life time $T_{life}$ can meet the delay requirement $D_{req}$, instead of a design-time timing constraint (i.e., $D_{path_i}$) at the design time can meet the delay requirement $D_{req} - \Delta D$, such that extra leakage savings can be achieved.

### III. Leakage and Delay Models Considering NBTI

In this section, we describe the leakage current model, NBTI-induced $V_{th}$ degradation model for PMOS, and NBTI-aware delay model as preliminaries for our NBTI-aware dual $V_{th}$ assignment technique. In this paper, a combinational circuit is represented by a Directed acyclic graph (DAG) $G = (V, E)$. A vertex $v \in V$ represents a CMOS gate from a given library, while an edge $(i, j) \in E$, $i, j \in V$ represents a connection from vertex $i$ to vertex $j$.

#### 1. Leakage current model

For all the gates in the given standard cell library, we create a leakage lookup table by simulating all the gates in the standard cell library under all possible input patterns. Thus the leakage current $I_{leak}$ can be expressed as:

$$I_{leak}(v) = \sum_{\text{input}} I(v, \text{input}) \times \text{Prob}(v, \text{input})$$

where $I(v, \text{input})$ and $\text{Prob}(v, \text{input})$ are the leakage current (including subthreshold and gate leakage current) and the probability of gate $v$ under input pattern input. We use 90nm PTM\cite{15}, in which the original $V_{th}$ of NMOS and PMOS are 220mV and ~220mV respectively. We also create leakage lookup tables for gates with higher $V_{th}$ ranging from 260mV to 420mV (every 10mV) for optimal high $V_{th}$ selection.

#### 2. NBTI-induced $V_{th}$ degradation model

An NBTI-induced threshold voltage degradation $\Delta V_{th}$, which is caused by the traps generated at the interface, can be expressed as\cite{8}:

$$\Delta V_{th} = (1 + m) q_t N_{it}(t)/C_{ox}$$

where $m$ represents equivalent voltage $V_t$ shifts due to mobility degradation, $q_t$ is the electronic charge, $C_{ox}$ is the gate oxide capacitance.

In this paper, our proposed fitting model is used\cite{16,17}, to calculate the $V_{th}$ degradation for different original $V_{th}$. Firstly the interface trap generation $N_{it}$ can be described as:

$$N_{it}(t) = 1.16 \times \sqrt{q_t N_{it0}/k_B T_i^1/4}$$

where $\xi(p_a) = p_a^{0.27p_a+0.28}$. Thus $V_{th}$ degradation is derived as:

$$\Delta V_{th} = \eta \times \sqrt{\frac{1}{(1 + p_a^{0.27p_a+0.28})} \times t^{1/4}}$$

and the parameter $\eta$ is decided by the predictive model proposed in Ref.\cite{4} which also assumed that $N_{it}$ is proportional to $t^{1/4}$:

$$\eta(V_{th}) = AT_{ox} \sqrt{C_{ox}(V_{gs} - V_{th})} \times \exp\left(\frac{E_{ox}}{E_0}\right) \exp\left(-\frac{E_v}{\frac{E_v}{k_B t}}\right)$$

which varies with different initial $V_{th}$. Although $\eta$ may degrade with time as the $V_{th}$ decreases, but the influence is very small. When you choose $V_{gs} = 1.0V$, $V_{th} = 200mV$, largest $\Delta V_{th} = 50mV$ after ten years, the $\eta$ ($t$=ten years)/$\eta(t = 0) \approx 97\%$. So we assume that $\eta$ only depends on the original $V_{th}$ at time 0.

#### 3. Delay model

The proportion delay $d_{V_{th}}(v)$ for high $V_{th}$ gate can be expressed as\cite{18}:

$$d_{V_{th}}(v) = \frac{K_C L V_{DD}}{(V_{DD} - V_{th})^n}$$

$$\approx d_{V_{th}} \times \left(1 + \alpha \frac{V_{th} - V_{thb}}{V_{DD} - V_{thb}}\right)$$

where $K_C$, $L$, $V_{DD}$, $V_{thb}$, $V_{th}$ are load capacitance at the gate output, the velocity saturation index, and the proportionality constant respectively.

According to Eq.(4) in the previous subsection, the NBTI-induced $V_{th}$ degradation will lead to gate delay degradations. Thus the worst case NBTI-aware delay of low $V_{th}$ gate $v$: $d_{V_{th}}^{N_{V_{th}}}(v, t)$, can be derived as:

$$d_{V_{th}}^{N_{V_{th}}}(v, t) \approx d_{V_{th}} \times \left(1 + \alpha \frac{\Delta V_{V_{th}}(v, t, p_a)}{V_{DD} - V_{thb}}\right)$$

where $\Delta V_{V_{th}}(v, t, p_a)$ is the $V_{th}$ degradation of low $V_{th}$ gate $v$ with duty cycle $p_a$ at time $t$.

Meanwhile, different original $V_{th}$ assignments lead to different $V_{th}$ degradation, the NBTI-aware delay of high $V_{th}$ gate $v$: $d_{V_{th}}^{N_{V_{th}}}(v, t)$ is described following Eqs.(4) and (6):

$$d_{V_{th}}^{N_{V_{th}}}(v, t) \approx d_{V_{th}} \times \left(1 + \alpha \frac{\Delta V_{V_{th}}(v, t, p_a)}{V_{DD} - V_{thb}}\right)$$
The NBTI-induced delay degradation of gate $v$ with low and high $V_{th}$ can be derived from Eqs.(6), (7), and (8):

$$\Delta d^N_{vthl}(v,t) = d_{vthl} \times \left( 1 + \frac{\alpha \Delta V_N(V_{thl}, t, p_s(v))}{V_{DD} - V_{thl}} \right)$$

and

$$\Delta d^N_{vthh}(v,t) = d_{vthh} \times \left( 1 + \frac{\alpha \Delta V_N(V_{thh}, t, p_s(v))}{V_{DD} - V_{thh}} \right)$$

We notice that the delay at a certain time point $t$ can be derived using our NBTI-aware delay model. Usually in the analysis of circuit NBTI-induced performance degradation, $t$ will be replaced by the lifetime requirement $3 \times 10^8$, which is about 10 years. Further our NBTI-aware delay model not only depends on the different original gate threshold voltage $V_{th}$ and the time point $t$, but also depends on the duty cycle $p_s(v)$, which is related to signal probabilities and the activity factors of the gate $v$. In this paper, the duty cycle $p_s(v)$ is derived by the gate input probability $Prob(v, input)$ using a circuit logic simulator. From the above equations, all the delays can be described using $d_{vthl}(v)$, which is extracted from the technology library.

IV. NBTI-aware Dual $V_{th}$ Assignment

In this section, we first formulate the NBTI-aware dual $V_{th}$ assignment as an Integer linear programming (ILP) problem to show the difference of the traditional methods and our NBTI-aware dual $V_{th}$ assignment method. Original dual $V_{th}$ assignment is with a delay target at time $0$; while NBTI-aware dual $V_{th}$ assignment is with a delay target at time $T_{life}$. Then we describe a heuristic algorithm to quickly solve the NBTI-aware dual $V_{th}$ assignment problem and obtain the optimal high $V_{th}$ for each circuit.

1. Problem definition

If the lifetime reliability is considered during the leakage optimization, the object function and timing constraints in previous deterministic ILP model should be changed accordingly. First of all, the leakage current varies due to NBTI-induced degradation of each gate. Since the NBTI-induced $V_{th}$ degradation only leads to a decreased leakage current after a certain time interval, the leakage current at time 0, which is the maximum leakage current, is still used as the object function:

$$I_{leak}(G,t)|_{t=0} = \sum_{v \in V} (I_{leak}^{v}(v,t) \times (1 - H(v))) + I_{leak}^{vth}(v,t) \times H(v)$$

Secondly, the required time leakage constraint $D_{req}$ changes into $D_{eqv}(T_{life})$, which is the required time of the circuit after a time interval of $T_{life}$. Here, $T_{life}$ represents the lifetime requirement. Therefore, the timing constraints change into:

$$t_a(m, n) = 0, \quad \forall m \in PI$$

$$t_a(n, t) + d(n, t) \leq D_{eqv}(T_{life}), \quad \forall n \in PO$$

$$t_a(i, t) + d(i, t) \leq t_a(j, t), \quad \forall (i, j) \in E, \quad i, j \in V$$

that means at every time point $t$ ($t \leq T_{life}$), these constraints should be always satisfied. $t_a(v, t)$ and $d(v, t)$ are the arrival time and gate delay of gate $v$ at time $t$.

Furthermore, according to Eqs.(7) and (8), the time dependent delay model should be changed to

$$d(v, t) = d_{vthl}(v) \times (1 - H(v)) + d_{vthh}(v) \times H(v)$$

$$= d_{vthl} \times \left( 1 + \frac{\alpha \Delta V_N(V_{thl}, t, p_s(v))}{V_{DD} - V_{thl}} \right) \times (1 - H(v)) + d_{vthh} \times \left( 1 + \frac{\alpha \Delta V_N(V_{thh}, t, p_s(v))}{V_{DD} - V_{thh}} \right) \times H(v)$$

In the timing analysis, $t_a(v, t)$ varies with $d(v, t)$ at any time $t \leq T_{life}$, the most critical constraints are the required time constraints at POs. Hence, if the timing constraints at time $t = T_{life}$ are satisfied, all the above constraints are satisfied. Therefore, our NBTI-aware dual $V_{th}$ assignment can be modeled as the ILP model in Fig.2. The required time $D_{eqv}(T_{life})$ should be larger than the max delay of the circuit at time point $T_{life}$. All the timing attributes of the circuit at different time points can be derived by a modified STA tool using our NBTI-aware delay model.

**Minimize:**

$$I_{leak}(G,t)|_{t=0} = \sum_{v \in V} (I_{leak}^{v}(v,t) \times (1 - H(v))) + I_{leak}^{vth}(v,t) \times H(v))$$

**Subject to:**

1. Timing constraints:

$$t_a(m, T_{life}) = 0, \quad \forall m \in PI$$

$$t_a(n, T_{life}) + d(n, T_{life}) \leq D_{req}(T_{life}), \quad \forall n \in PO$$

$$t_a(i, T_{life}) + d(i, T_{life}) \leq t_a(j, T_{life}), \quad \forall (i, j) \in E, \quad i, j \in V$$

2. Gate constraint:

$$d(v, T_{life}) = d_{vthl}(v) \times (1 - H(v)) + d_{vthh}(v) \times H(v), \quad \forall v \in V$$

**Variable constraints:**

$H(v)$ are binary variables

**Fig. 2. ILP model for our NBTI-aware dual $V_{th}$ assignment**

2. Our heuristic algorithm

One of the major bottlenecks of using the ILP method is the computation complexity. Although the ILP model leads to an optimal result, it cannot be used in a real design cycle because of the computation complexity for large circuits. In this subsection, we propose a fast and accurate heuristic algorithm shown in Fig.3, to speed up the dual $V_{th}$ assignment with a near optimal result.

A DAG pruning method[19] is used to reduce the problem size (Line 1 to Line 4 in Fig.3), where $t_{arr}(v)$ is the arrival time from POs to $v$, $G_{ker}$ is the pruned DAG. If all the gates in the circuits are assigned to high $V_{th}$ gates, the critical path delay $D_{max}$ may violate the timing constraint $D_{req}$. However, there may be some paths in the circuit can still satisfy the performance constraints. Some gates in such paths can be deleted from the DAG without affecting the timing constraints. We define $T_{path}(v)$ as the path delay of the longest path that including gate $v$. Therefore, if $T_{path}(v) \leq D_{req}$ when high $V_{th}$ is assigned to each gate, gate $v$ does not affect the circuit performance constraint whether gate $v$ is assigned with high $V_{th}$ or not; thus this gate $v$ can be pruned. In Line 5 of Fig.3, we use a greedy algorithm proposed in Ref.[20] to assign high $V_{th}$ gates as many as possible in the pruned DAG.

V. Implementation and Experimental Results

This section describes the implementation and shows the experimental results for ISCAS85 benchmark circuits. The simulation results are based on a standard cell library constructed using the PTM 90nm bulk CMOS model[15]. $V_{dd} = 1.0V, |V_{thl}| = 220mV are
set for all the transistors in the circuits. The circuit lifetime requirement $T_{th}$ is set to be $3 \times 10^8$ s (about 10 years). The temperature is set to 400K. The leakage current lookup tables (including both subthreshold and gate leakage current) are created using HSPICE and PTM 90nm bulk CMOS model. All ISCAS85 benchmark circuit netlists are synthesized using a commercial synthesis tool and mapped to the 90nm standard cell library. A Static timing analysis (STA) tool [21] is modified to calculate the circuit performance degradation, with the usage of our NBTI-aware delay model. We simulate 10k input vectors using a zero delay simulator and get the degradation, with the usage of our NBTI-aware delay model. We simulate 10k input vectors using a zero delay simulator and get the degradation, with the usage of our NBTI-aware delay model.

First the gate number decreases about 49.4% after the DAG pruning algorithm, and 52.1% considering the NBTI effect. The path delay constraint $D_{req}$ changes and the delay variation of high $V_{th}$ gate due to NBTI effect is less than that of low $V_{th}$ gate, hence the probability of $T_{path} (v) \geq D_{req}$ becomes smaller in Line 3 of Fig.3. Secondly, our NBTI-aware dual $V_{th}$ assignment can assign more high $V_{th}$ gates ($N_{th} > N_H$). Finally, due to more high $V_{th}$ gates in the circuit, our NBTI-aware dual $V_{th}$ assignment leads to on average 3.46% more leakage saving while ensures the lifetime requirement. For circuit C432, the improvement of leakage reduction rate reaches up to 14.88%. The improvement of leakage reduction rate using our NBTI-aware dual $V_{th}$ without performance relaxation is about 1.19%.

1. Degradation analysis with different $V_{th}$

The comparison of the PMOS and circuit performance degradation with different original $V_{th}$ is shown in Fig.4. When $V_{th} = 220$mV, the largest difference of $V_{th}$ degradation and circuit performance degradation is about 10%; when $V_{th} = 320$mV, this difference decreases to about 3%; when $V_{th} = 420$mV, the PMOS $V_{th}$ and the circuit performance degrades at nearly the same speed. Also, we can see that higher $V_{th}$ leads to more circuit performance degradation at earlier time points, but finally becomes less than the lower $V_{th}$ condition. Referring to Eqs.(9) and (10), at first the difference of $V_{th}$ degradation $\Delta \psi (V_{th}(t), p_n(v))$ is small with different original $V_{th}$ while $\Delta \psi (V_{th}(t) = V_{thh})$ is smaller than $\Delta \psi (V_{th}(t) = V_{thl})$, thus the delay degradation $\Delta \psi^N_{thh} (v,t)$ is larger than $\Delta \psi^N_{thl} (v,t)$). Therefore the circuit performance degradation with higher $V_{th}$ gates is larger. With time goes by, the difference of $\Delta \psi (V_{th}(t), p_n(v))$ and $\Delta \psi (V_{th}(t) = V_{thh})$ becomes larger, the delay degradation $\Delta \psi^N_{thh} (v,t)$ becomes larger than $\Delta \psi^N_{thl} (v,t)$, thus the performance degradation of circuits with lower $V_{th}$ gates exceeds that of circuits with higher $V_{th}$ gates. This can be seen more clearly in Fig.5 in the following subsection.

In Fig.4, after about $10^8$s, a higher $V_{th}$ leads to less circuit performance degradation compared with a lower $V_{th}$. Thus it may be possible to assign more high $V_{th}$ gates in the path, if the path delay constraints change in order to ensure the lifetime requirement (larger than $10^8$s).

2. Results for NBTI-aware dual $V_{th}$ assignment

(1) Fixed high $V_{th}$

We use a fixed high $V_{th} = 320$mV to compare the previous and NBTI-aware dual $V_{th}$ assignment under 5% circuit performance relaxation in Table 1. $N_G$ is the total gate number, $N_r$ is the gate number of reduced DAG after DAG pruning algorithm, $N_H$ is the total high $V_{th}$ gate number after assignment, $I_{leak}$ is the leakage current after dual $V_{th}$ assignment.

First the gate number decreases about 49.4% after the DAG pruning algorithm, and 52.1% considering the NBTI effect. The path delay constraint $D_{req}$ changes and the delay variation of high $V_{th}$ gate due to NBTI effect is less than that of low $V_{th}$ gate, hence the probability of $T_{path} (v) \geq D_{req}$ becomes smaller in Line 3 of Fig.3. Secondly, our NBTI-aware dual $V_{th}$ assignment can assign more high $V_{th}$ gates ($N_{th} > N_H$). Finally, due to more high $V_{th}$ gates in the circuit, our NBTI-aware dual $V_{th}$ assignment leads to on average 3.46% more leakage saving while ensures the lifetime requirement. For circuit C432, the improvement of leakage reduction rate reaches up to 14.88%. The improvement of leakage reduction rate using our NBTI-aware dual $V_{th}$ without performance relaxation is about 1.19%.

Further, the circuit degradation comparison of C1908 without performance degradation is shown in Fig.5 to illustrate the impact of our NBTI-aware optimization on circuit performance degradation with time. The original dual $V_{th}$ assignment with a delay target at time 0 does not change the critical path, thus the circuit performance degradation is just the same as the original circuit with all low $V_{th}$ gates: there is no high $V_{th}$ gates in the critical path of the circuit after original dual $V_{th}$ assignment. Before time $t_0$, the performance degradation of circuit after NBTI-aware dual $V_{th}$ assignment with delay target at $t = t_{th}$ is almost the same as that of the circuit with all high $V_{th}$ gates, and is larger than that of the circuit after the original dual $V_{th}$ assignment. After time $t_0$, the performance degradation after NBTI-aware dual $V_{th}$ assignment is larger than that of the circuit with all high $V_{th}$ gates, and follows the increasing trend of the degradation of circuit after the original dual $V_{th}$ assignment.

Our NBTI-aware assignment leads to a larger delay at time 0.
and a equal delay at time $T_{thf}$. Our NBTI-aware assignment is different with an original assignment with a delay target equal to the initial (at $T = 0$) delay of our NBTI-aware assignment, because in our NBTI-aware assignment, the gates that assigned with high $V_{th}$ not only depend on $\Delta$leakage/$\Delta V_{th}$ but also depend on their sensitivity to the NBTI effect.

(2) Optimal high $V_{th}$ selection

We also select the optimal high $V_{th}$ without performance relaxation for each ISCAS85 benchmark circuit. Table 2 shows that our NBTI-aware dual $V_{th}$ assignment leads to different optimal high $V_{th}$ and further leakage reduction: on average 3.44%. $I_{ori}$ is the original circuit leakage before any optimization. $R_{ori}$ and $R_{X}$ are the leakage reduction rate for original and our NBTI-aware dual $V_{th}$ assignment. Notice that the optimal high $V_{th}$ $V_{thh}^{NBTI}$ is always equal or greater (on average 11mV higher) than the optimal $V_{th}$ in original dual $V_{th}$ assignment.

The effect of NBTI-aware optimization varies with circuits as shown in Table 2. The leakage current reduction varies a little with circuits that have a uniform (or balanced) path delay distribution, such as C499 and C3555. For some other circuits with unbalanced path delay distribution, such as C880, C2670, and C3540, the improvement in leakage reduction can be up to 7.32%.

Table 2. Optimal $V_{th}$ selection without performance relaxation

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<th>$I_{ori}$ (nA)</th>
<th>$V_{th}$ (mV)</th>
<th>$V_{thh}^{NBTI}$ (mV)</th>
<th>$R_{ori}$ (%)</th>
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<td>4407.8</td>
<td>350</td>
<td>360</td>
<td>12.17</td>
<td>11.47</td>
<td>5.68</td>
</tr>
<tr>
<td>average</td>
<td>$\Delta V_{thh} = 11$</td>
<td>19.03%</td>
<td>18.23%</td>
<td>3.44%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VI. Conclusion and Future Works

In this paper, we study the dual $V_{th}$ assignment techniques with the consideration of circuit aging effect caused by NBTI. Based on the fact that gates with lower $V_{th}$ tend to age faster, while gates with higher $V_{th}$ has a slower degradation[4], we develop a delay degradations model and propose a new dual $V_{th}$ assignment algorithm, such that extra leakage savings can be achieved. The experimental results on ISCAS85 for 90nm technology show that the NBTI-aware dual $V_{th}$ assignment technique assigns more high $V_{th}$ gates in the circuits and may change the critical paths, as long as the performance during the product lifetime can still meet the timing constraints. Our NBTI-aware dual $V_{th}$ assignment is not only depend on $\Delta$leakage/$\Delta V_{th}$ but also depend on their sensitivity to the NBTI effect. From physical mechanisms to modelling", Microelectronics Reliability, Vol.46, No.1, pp.1–23, 2006.


References

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