Design of Sparse Mesh for Optical Network on Chip

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ABSTRACT

Nanoscale CMOS technologies are posing new network on chip concepts to IC designers. However, the electronic network on chip design faces many problems like energy consumption, long delay and limited bandwidth. Hence, optical network on chip appears as a good candidate to solve these problems. The advances in nanophotonic technology make it more realistic. A new sparse mesh is proposed for optical network on chip. Two types of non-blocking optical node architecture are also proposed to build up core node and switch node. The new architecture fully utilizes the property of XY routing in 2D mesh network, thus saving the number of microring resonators used. The comparisons are made with traditional mesh in number of microring resonators, loss and energy. The results show that the proposed sparse mesh achieves the best in all the aspects. For example, it uses 68% less number of resonators than the traditional mesh. We simulated 2D sparse mesh optical network on chip, and showed network performance under different traffic loads and data sizes. The results show sparse mesh achieves lower average delay and higher throughput than the traditional mesh.

Keywords: Optical Interconnect, network on chip, mesh, router architecture

INTRODUCTION

The advance of semiconductor technology enables the number of transistors in a single chip increases to billions or even larger numbers. Traditional on-chip communication techniques for SoC face several issues, such as poor scalability, limited bandwidth, low utilization, and so on. Networks-on-chip (NoCs) promise to relieve these issues by modern communication and networking theories [1][2]. Many NoCs have been proposed, such as Dally’s NoC [3], Nostrum [4], ASNoC [5], and etc. However, as semiconductor technologies continually scale the feature sizes down and the on-chip communications required by new applications increases, the conventional metallic interconnect is becoming the bottleneck of NoC performance with limited bandwidth, long delay, and high power consumption. Therefore, electronic NoC may not satisfy future bandwidth and latency requirement within the power consumption budget [6][7][8].

Optical NoC (ONoC) is based on optical interconnect and is a promising candidate to overcome these limitations. Before applied to NoC, optical interconnect has demonstrated its strengths in multicomputer systems, on-board inter-chip interconnect, and switching fabrics in Internet routers. Router is the basic unit to build an interconnection network. Several node architectures for optical network on chip, which are based on microring resonators [8], are proposed in literature. λ-router is proposed in [9], which uses N wavelengths and multiple basic 2x2 switching elements to realize NxN non-blocking switching function. Another non-blocking node is proposed in [10]. It is based on a 2x2 switching element design to implement a 4x4 node. Since typical 2D NoCs use 5x5 nodes, the 4x4 node is augmented by extra components for local injection and ejection. It is an improvement over the previous design [11]. The improved node architecture optimizes the architecture and solves the blocking issue.

With node architectures available, interconnection networks can be built up by connecting nodes in a certain way. Mesh topology is a popularly used for network on chip. It consists of a grid of horizontal and vertical lines with nodes placed at their intersections. Its simple layout makes the application of minimal routing easily. However, the performance of mesh is limited. In this paper, we propose a new sparse mesh for optical NoCs using XY routing algorithm. In XY routing, each packet is routed first in X dimension until it reach the node, which is in the same column with the destination, and then along the perpendicular Y dimension to the destination. XY routing is a minimal path routing algorithm and is free of deadlock and livelock. In addition, it is a low-complexity distributed algorithm without using any routing table. These features make XY routing algorithm particularly suitable for NoCs, which require low latency and low cost at the same time. Many practical systems have been using it [12], and it has also been favored by many NoC studies [10][11] [13][14][15][16].

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Compared with traditional mesh (Tmesh), sparse mesh (Smesh) consists of two types of nodes, i.e. core node and switch node. New architectures for core node and switch node are designed respectively. Smesh requires less number of microring resonators, consumes less power, and has lower optical power loss. It has been designed to take advantages of the properties of XY routing. To save power and reduce optical power loss, the microring resonators of a Smesh are active only when packets need to make turns.

**OPTICAL SPARSE MESH NETWORK ON CHIP NETWORK ARCHITECTURE**

![Diagram of 6x6 optical sparse mesh network on chip.](image)

The architecture of our proposed sparse mesh topology is shown in Figure 1. The sparse mesh ONoC consists of two overlapped networks, an optical network for large payload packets and an electronic network for control packets and small payload packets. Payload packets carry data and processor instructions, while control packets carry the network control information. The electronic network connects the control units of all the nodes in the same topology as the optical network. In general, the topologies of the two networks can be different. For example, torus can be used for the optical network by adding a waveguide to each pair of end routers. The optical and metallic interconnects are all bidirectional. While the optical interconnects are 1-bit wide on each direction, metallic interconnects are 32-bit wide on each direction.

Different from the Tmesh, Smesh consists of two types of nodes, i.e. core node and switch node. The core nodes are connected to the IP cores. They can inject, eject and also relay the information. Switch nodes don’t connect to IP cores and they only have function of relay information. In the following, we will show our new architectures for these two nodes in details.

Optical routers are the key components of the nodes in optical NoC. They implement the routing and flow control functions. An optical router switches packets from an input port to an output port using a switching fabric, which is composed of multiple basic switching elements. We proposed two types of new optical router architectures for optical sparse mesh NoCs based on XY routing algorithm, as are shown in Figure 2 (a) and (b). It consists of a switching fabric and a control unit which uses electrical signals to configure the switching fabric according to the routing requirement of each packet. In both core node and switch node, the control unit is built from traditional CMOS transistors and uses...
electrical signals to power on and off each microring resonator. The control units of all the nodes in a sparse mesh optical NoC use an electronic network to setup and maintain optical paths.

The switching fabric is built up by microring resonators (MRs), which have the same on-state and off-state resonance wavelengths, $\lambda_{on}$ and $\lambda_{off}$. Figure 2(c) show how optical signals are transferred in both On and Off states with different positions of the waveguides. The optical signals use a single wavelength which corresponds to $\lambda_{on}$. The on-off state change of MR will guide the optical signals to different ports. The switching fabric of the switch node implements a 4x4 switching function, which uses only 4 microring resonators and 4 waveguides. The core node is a little complex because of the connection to the IP core. Hence, the switching fabric of core node implements a 5x5 switching function, which uses only 12 microring resonators and 6 waveguides. We can also replace the last resonator on the waveguide for the injection port with Y branch. Although this reduced the number of resonators and save power, more loss will be encountered by packets which exist from the east port. Compared with the crossbar, it uses not only the basic 1x2 switching elements with the crossing structure, but also those with the parallel structure to reduce the waveguide crossing insertion loss. Furthermore, the internal structure of the switching fabric is designed to avoid waveguide crossings.

Both core node and switch node have an excellent feature, i.e. regardless of the network size, the maximum power to route a packet through a 2D sparse mesh NoC is a constant number. This feature is especially helpful for large networks and network scalability. The feature is designed by avoiding any resonator switching activity for routing packets between the two horizontal ports and the two vertical ports inside the node. It means that at most three nodes need to power on one resonator for any packet in a network of any size.

For optical NoCs using XY routing algorithm, both core node and switch node are strictly non-blocking. This can be proved by listing all the possible cases. For example, when a packet is injected from injection port to the east port, it will not block packets from west to south, or west to north, or south to north, or north to south. Some cases are not allowed by XY routing algorithm, such as that turns from south/north to east/west.

![Fig. 2. Router architectures for core node and switch node](image-url)
COMPARISON AND ANALYSIS

We compared the sparse mesh network on chip, built from core nodes and switch nodes, with the traditional mesh built from crossbar based nodes. We compared and analyzed three main aspects, including the power consumptions, optical power insertion losses, and areas in terms of the numbers of microring resonators.

The number of microring resonators used by an optical mesh NoC decides its area cost along with its floorplan. Lower number of resonators indicates a lower chip cost by reducing die size and increasing yield. We compared the numbers of resonator required to build optical mesh NoC of different sizes by the Smesh and Tmesh in Figure 3. Smesh uses the lower number of resonators than the Tmesh. As the network scales, this gap becomes broader.

![Fig. 3. Comparison of numbers of microring resonator used under various network sizes](image)

Power consumption is a critical aspect of ONoC design. For high-performance computing, low power consumption can reduce the cost related with packing, cooling solution, and system integration. Optical NoCs consume power in three ways. First, ONoC interfaces consume power to generate, modulate, and detect optical signals. Second, optical routers consume power to route packets. Third, the networked control units of an ONoC consume power to communicate and process routing information. We are concentrated on the second item and assume the Smesh and Tmesh use the same networked control units and network interfaces for XY routing algorithm.

Due to the asymmetrical architecture of an optical router, a packet taking different input and output ports will require different amount of power to route it. To better measure the power efficiency of the optical routers, we analyzed the average power consumption of a path in the 2D mesh NoC. The average power consumption per optical path $E_p$ is calculated using the equation (1). $M$ is the total number of optical paths in a network. $E_i$ is the power consumed on the $i$-th path when the bandwidth is $B$.

$$E_p = \frac{\sum_{i=1}^{M} E_i}{M \times B}$$

We assume a moderate bandwidth of 12.5Gbps for each path in the network. An optical router needs to power on and off its microring resonators to route packets. In the on state, the microring resonator need a DC current and consume less than 20µW [17]. In the off-state, no power will be consumed by a microring resonator, if we ignore the small bias.
voltages to mitigate process variations. The power consumption of the resonator is expected to decrease with continual improvement of its material and internal structure.

As Figure 4 shows, regardless the size of a network, Smesh has constant average power consumption per path. This is due to the optimized architecture and can be explained as follows. According to the architecture of core node and switch node, Smesh does not need to power on any resonator for a packet traveling along a column or row. Smesh only powers on one resonator when a packet enters a network from an injection port, turns from a row to a column, or exits the network from an ejection port. In the worst case, at most three resonators are powered on to route a packet in a Smesh, and this number does not change with the network size. This feature allows an optical network based on Smesh scales without worrying the power consumed by the additional nodes on a longer path. In comparison, Smesh based ONoC scales better than Tmesh.

![Fig. 4. Comparison of power per path under various network sizes](image)

Optical power loss of an ONoC decides its feasibility as well as the power consumption. In our comparison, we considered two major sources of optical power losses, the waveguide crossing insertion loss and microring resonator insertion loss. The waveguide crossing insertion loss is 0.12dB per crossing, and the microring resonator insertion loss is 0.5dB [18]. We compared the maximum loss, minimum loss, and average loss of all possible cases (Table 1). Core node has 28% less minimum loss, 27% less average loss, and 33% less maximum loss than the crossbar based node. And switch node achieves even lower average, maximum and minimum loss.

<table>
<thead>
<tr>
<th></th>
<th>Average</th>
<th>MAX</th>
<th>MIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crossbar based node</td>
<td>0.98</td>
<td>1.46</td>
<td>0.50</td>
</tr>
<tr>
<td>Switch node</td>
<td>0.43</td>
<td>0.74</td>
<td>0.24</td>
</tr>
<tr>
<td>Core node</td>
<td>0.72</td>
<td>0.98</td>
<td>0.36</td>
</tr>
</tbody>
</table>

We also compared the average loss of the longest paths in the 8x8 Smesh and Tmesh NoC. If we mark the nodes in the four corners as node (0, 0), (0, 7), (7, 0), and (7, 7) respectively in the 8x8 Smesh and Tmesh NoC, the longest paths for XY routing algorithm are between node (0, 7) and (7, 0). We analyzed the longest path loss for Smesh and Tmesh similarly. For Smesh, a packet is sent from node (0, 7) to (7, 0). The packet enters NoC from the injection port to the east port, and encounters four waveguide crossings and one resonator. So the loss is 0.12x4+0.5=0.98dB. In the second node
(1, 7) on the path, two waveguide crossings are encountered, so the loss is 0.12x2=0.24dB. This is the same case for the following two switch nodes (3, 7), (5, 7). In the third node (2, 7) on the path, three waveguide crossings are encountered, so the loss is 0.12x3=0.36dB. This is the same case for the following two core nodes (4, 7), (6, 7). In the corner node (7, 7), one resonator is encountered, so the loss is 0.5dB. Similarly, there are four crossings in node (7, 6), (7, 4), and (7, 2) each, so the loss is 0.12x4=0.48dB. There are two crossings in node (7, 5), (7, 3), and (7, 1) each, so the loss is 0.12x2=0.24dB. At the destination node (7, 0), one resonator is encountered, so the loss is 0.5dB. Therefore, the total loss in the longest path is to 5.94dB. The calculation for the path from node (7, 0) to (0, 7) is similar with the same value obtained. Hence, the average loss for the longest path in Smesh is 5.94 dB. And the result of 14.7dB is obtained in the similar way for the longest path in Tmesh. Smesh has the lower loss than Tmesh in this comparison. Smesh has 60% less longest path loss than the Tmesh.

**SIMULATION RESULTS**

We built 2D sparse mesh ONOC using core node and switch node and studied its performance. XY routing algorithm is used in the simulation. In the optical NoC, processors generate packets independently and at time intervals following a negative exponential distribution. We used the uniform traffic pattern, i.e. each processor sends packets to all other processors with the same probability. The ONOC is simulated using a network simulator, OPNET [19].

The performance of the ONOC is measured in terms of end-to-end (ETE) delay and throughput. The ETE delay is the average time between processors generating packets and the packets reaching destinations. It is the sum of the connection-oriented path-setup time and the time used to transmit optical packets. We simulated 8x8 network size and use the 32-bit, 32-bit size for path-setup and acknowledge packets respectively.

![Fig. 5. ETE delay vs. Offered Load with Smesh and Tmesh](image)

The performance of ETE delay with two different data sizes, 64 and 128 bytes, are compared in Figure 5. For the same data packet size, Smesh achieves lower ETE delay and saturates later than Tmesh. For example, Smesh saturates at the offered load of about 0.29 for 128 bytes size, while Tmesh saturation load is about 0.16. The improvement owes to the provision of the intermediate switch nodes which alleviate the traffic load in each dimension. It can also be seen that, for Smesh or Tmesh, smaller data packet size suffers from more serious degradation in performance. More packets will be generated for the small data packet size network. Serious contentions for limited resources lead to performance degradation. Figure 6 shows the network throughput under different offered load of Smesh and Tmesh using the different data packet sizes. The trend concluded from ETE delay can be obtained more clearly here.
CONCLUSION

We proposed a new optical sparse mesh for network on chip, which uses XY routing algorithm. Two types of node architectures are designed to build up the sparse mesh. Smesh NoC is compared with Tmesh and the comparison results show that Smesh has the lowest power consumption and losses and requires the smallest area. Smesh can guarantee the maximum power to route a packet through a network to be a small constant number, regardless of the network size. We simulated 8x8 2D sparse meshes and traditional mesh NoCs based on XY routing algorithm, and showed the end-to-end delay and network throughput under different load and data sizes.

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