A 5-GHz-Band CMOS Receiver With Low LO Self-Mixing Front End

Hsiao-Chin Chen, Member, IEEE, Tao Wang, Hung-Wei Chiu, Yu-Che Yang, Tze-Huei Kao, Guo-Wei Huang, Member, IEEE, and Shey-Shi Lu, Senior Member, IEEE

Abstract—A 5.0-GHz-band monolithic direct-conversion receiver front end employing subharmonic mixers (SHMs) is demonstrated in 0.18-μm CMOS technology. Instead of using transistors as transconductors, the SHMs adopt on-chip 1:4 transformers to achieve voltage gain, and hence, excellent local-oscillator self-mixing suppression and good linearity can be obtained. Additionally, a CMOS-compatible postprocess is used to selectively remove the silicon substrate underneath the inductors and transformers of the receiver front end. While dissipating 43.9 mW from a 1.8-V supply, the micromachined receiver front end exhibits a voltage gain of 28.0 dB, a noise figure of 9.7 dB, a third-order input intercept point of $-7.8$ dBm at 5.0 GHz, and an input-referred dc offset of $-118.0$ dBm. The proposed receiver front end is further integrated with analog baseband circuits, a fractional-N frequency synthesizer, and a serial-to-parallel data converter to accomplish a multioperation-mode receiver.

Index Terms—CMOS, direct conversion, front end, local-oscillator (LO) self-mixing, quadrature coupler, receivers, subharmonic mixers (SHMs), transformers.

I. INTRODUCTION

OWADAYS, the direct-conversion configuration [1] has become the most popular architecture in commercialized wireless transceiver integrated circuits. However, directly down-converting the received radio-frequency (RF) signals to zero frequency makes the receiver very susceptible to the dc offset. This is because the magnitude of the dc offset at the mixer output may be several tens of decibels larger than that of the desired signal and the circuits following the mixer will be saturated by such offset voltage, which inevitably retards the signal amplification [2].

One of the mechanisms that cause dc offsets, perhaps the most troublesome one, is the self-mixing phenomenon of local-oscillator (LO) signals in the direct-conversion receiver. A variety of subharmonic mixers (SHMs) have been reported to mitigate this problem [3]–[8]. However, scrutiny of these papers reveals that all these SHMs adopt transistors as transconductors. To achieve good linearity, monolithic transformers can be used to replace transistor transconductors in the mixers as was pointed out in [9] that a mixer with a transformer-coupled input has the potential to be highly linear. Moreover, the transformer-coupled mixer can operate at a low supply voltage since the number of stacked transistors is reduced compared with that of a conventional mixer [10]. In this work, transformer-coupled SHMs are utilized in the RF front end to achieve low LO self-mixing dc offset and good linearity.

Because a simple 90° phase splitting of the subharmonic LO signal is insufficient to realize receivers with in-phase/quadrature outputs, complex octet-phase generation techniques were applied to the subharmonic LO signal in [4], [5], and [7]. However, the excess power consumed in the octet-phase generation circuits seems to make this topology less attractive. In this work, the RF path quadrature generation technique is adopted instead of the octet-phase generation of the subharmonic LO signal. The traditional polyphase network for the quadrature generation certainly causes considerable signal loss in the RF signal path [11]. Therefore, in this work, we use a quadrature coupler to generate the required 90° in the RF path. Quadrature couplers have been used as quadrature phase generators in monolithic millimeter-wave circuits realized in GaAs technologies for their broadband characteristic [12]. The design and realization of a quadrature coupler at 2 GHz on a nonstandard high-resistivity silicon substrate has also been reported elsewhere [13]. However, these previous works still leave the IC design community doubts about realizing quadrature couplers in standard CMOS technologies due to the notorious silicon substrate losses. Lately, a quadrature mixer at 5 GHz on a standard silicon substrate has been designed and integrated into a receiver front end successfully [14], which clearly dispels such doubts.

In this paper, a direct-conversion receiver comprising a low noise amplifier (LNA), a quadrature coupler, transformer-coupled SHMs, analog baseband circuits (ABBs), and a frequency synthesizer is presented. This receiver was implemented in standard commercial 0.18-μm CMOS technology. In Section II, the proposed receiver architecture will be described. Then, in Section III, the design of the building blocks will be addressed. The measured results of the implemented circuits will be reported in Section IV followed by a summary in Section V.

II. RECEIVER ARCHITECTURE

The block diagram of the proposed direct-conversion receiver is shown in Fig. 1. The differential LO signals generated...
by the 2.45–3.1-GHz fractional-N frequency synthesizer are converted into 0°, 90°, 180°, and 270° signals required for the double-balanced SHM by a traditional polyphase filter. As previously mentioned, a simple 90° phase splitting of the subharmonic LO signal can only generate differential outputs in SHMs, and hence, an on-chip quadrature coupler is adopted for the quadrature generation in the RF path to get rid of the complex octet-phase generation in the LO path. Connected behind a single-ended LNA, the quadrature coupler splits the RF input signal into two signals in quadrature which are then converted into the differential signals by the transformers at the inputs of the two transformer-coupled SHMs. Mixed with the LO in the SHMs, these signals will be downconverted and then passed to the ABBs where the in-band signals are further amplified while the out-band signals are effectively rejected.

III. CIRCUIT DESIGN

A. LNA

The two-stage LNA is shown in Fig. 2. In the first stage, the cascode configuration is adopted to offer good isolation and frequency response. With proper device selection for the input transistor and matching elements, broadband input impedance matching and low-noise performance can be achieved simultaneously [15], [16]. In our design, the size of the input NMOSFET is 105/0.2 μm; the gate inductor $L_g$ and source inductor $L_s$ are 3.78 and 0.28 nH, respectively.

Since the LNA will be followed by the quadrature coupler, the output impedance of LNA should be matched to the coupler’s characteristic impedance which is 50 Ω in our design. Therefore, a source follower is chosen as the output stage of the LNA to facilitate the impedance transformation. Note that an n-type accumulation mode varactor is shunted between the output node of the cascode amplifier and the virtual ground node to contribute a variable capacitance at the output node of the cascode stage so that the tank resonant frequency can be varied by a control voltage. Thus, the peak-gain frequency at which the gain is maximal can be changed in order to provide sufficient gain over a wide frequency range. In other words, the operation frequency can be flexibly manipulated to meet the system requirement by applying a proper control voltage to the varactor.

B. Transformer-Coupled SHM

The principle of the proposed transformer-coupled SHM is explained in Fig. 3 [17]. The SHM is derived from the conventional Gilbert mixer in two steps. First, the differential pair used as the transconductor in the Gilbert mixer is replaced by 1:4 transformers which provide voltage gain and the single-ended-to-differential (StoD) conversion. Second, each transistor in the switching quad of the conventional Gilbert mixer is replaced by two transistors with their channels connected in parallel and their gates driven by a pair of differential LO signals. The parallel-connected transistors function analogously as an OR, and thus, the RF signal is mixed effectively with a signal having twice the LO frequency. Since the transformers provide the StoD conversion, the LNA and quadrature coupler in Fig. 1 are implemented in single-ended configuration so that the power consumption and the chip area can be reduced. The chip area of the two 1:4 transformers, the quadrature coupler, and the LNA are $210 \times 186 \times 2$, $423 \times 423$, and $620 \times 460 \ μm^2$, respectively. If the LNA and the quadrature coupler are implemented in differential configuration rather than in a single-ended one, the transformer’s chip area of 0.078 mm$^2$ can be saved but the chip area for the LNA and the quadrature coupler will grow by 0.464 mm$^2$, which means that the total chip area will increase by 0.386 mm$^2$.

As previously mentioned, the transformer with a step-up turn ratio is used as a voltage amplification element in the SHM. It seems that the turn ratio can be increased to achieve a large voltage gain. However, considerable loss can be introduced by the growing parasitic capacitances of the metal lines due to the increased number of turns. In this work, the SHMs employ 1:4 transformers to demonstrate a gain of 10.8 dB.

C. ABBs

The block diagram of the ABB is shown in Fig. 4 [18]. The main function of an ABB is to provide low-pass filtering and amplification to the downconverted baseband signals. Therefore, the ABB is basically a high-order low-pass filter (LPF) with
voltage gain. In this work, a Chebyshev type of seventh-order LPF is adopted as its frequency response has a steeper attenuation above the cutoff frequency than other types of filters. Based on a cascade topology, the seventh-order Chebyshev LPF is formed from a first-order gm-C filter and three biquads, as shown in Fig. 4. The Tow–Thomas biquad topology is employed as shown in Fig. 5. Because differential operational amplifiers (OPs) are utilized, the inverter in the original invention is dispensed by forming each feedback loop with the corresponding out-of-phase output of the second OP. To attain a robust and flexible system, digital calibration techniques are well used. A 7-bit successive-approximation-register-based analog-to-digital converter (SAR-ADC) is incorporated with a 7-bit digital-to-analog converter current array to achieve the dc-offset cancellation while an autotuning loop (ATL) provides an automatic bandwidth adjustment for the LPF.

The block diagram of the ATL is shown in Fig. 6. A biquad, acting as the master filter, cooperates with the charge-pump phase-frequency detector (CP-PFD) and another 5-bit SAR-ADC to form the ATL core. Theoretically, when a signal passes through a biquad, this signal would gain a 90° phase delay if it operates at the pole frequency of this biquad. Based on such an idea, if a reference signal at the desired corner frequency is applied to a biquad, we can examine the filter bandwidth by observing the phase delay contributed by the biquad. A divide-by-four circuit is used to provide a pair of I/Q signals at the pole frequency. The in-phase signal
will pass through the master filter and gain a certain phase delay around 90°. With this phase delay, the signal turns to be a quasi-quadrature signal which would be compared in the CP-PFD with the original quadrature signal generated by the divide-by-four circuit. The phase difference of these two signals would be converted into a logic high/low signal via a comparator. According to this logic signal which carries the phase difference information, the SAR-ADC would manipulate the digitally controlled cap arrays in the master/slave filter and simultaneously adjust the filter bandwidth [18].

In addition, the ABB can be operated at several different modes of operation. For example, three bandwidth options, namely, 5, 10, and 20 MHz, are provided to meet the different bandwidth requirements in wireless local area network (WLAN) applications. Furthermore, there are five gain settings to achieve a larger dynamic range. The bandwidth/gain control is accomplished by manipulating the internal memory through a three-wire interface (TWI) (clock/data/latch enable).

D. Frequency Synthesizer

The block diagram of the fractional-N frequency synthesizer composed of a CP-PFD, a voltage-controlled oscillator (VCO), a divider, and a $\Delta \Sigma$ modulator is shown in Fig. 7 [19]. The frequency synthesizer is intended to provide the LO signal to the SHMs. The overall tuning range of the 2.45–3.1-GHz cross-coupled CMOS VCO is accomplished by a binary-weighted capacitor array in parallel with a pMOS varactor. Employing a $\Delta \Sigma$ modulator, fractional-N division is realized in the frequency synthesizer to achieve an ultrafine frequency resolution (2 Hz).

In the proposed frequency synthesizer, CP current compensation is incorporated so that the reference spur can be suppressed. Switched-cap arrays are utilized in order to achieve low phase noise and a wide frequency range. In addition, through a set of control circuits, the bit number of a programmable frequency divider can be manipulated to extend the modulus range.

In particular, the MASH3 $\Delta \Sigma$ modulator is reduced by dumping the redundant hardware of its originator which is a cascade of three accumulators of 24 bits, but actually, the second and third stages need not have so many bits as the first stage does to deal with the quantization noise. The second and third stages in a conventional MASH3 $\Delta \Sigma$ modulator are truncated to 16 and 8 bits, respectively. Thus, 1/3 of the die area of the $\Delta \Sigma$ modulator can be saved while the reduced $\Delta \Sigma$ modulator is still comparable to the conventional $\Delta \Sigma$ modulator.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. RF Front End

The proposed RF front end consisting of an LNA, a quadrature coupler, and transformer-coupled SHMs was fabricated in 0.18-μm CMOS technology; moreover, a selective removal of the silicon substrate underneath the inductors [15] was applied to the chips through an inductively coupled plasma (ICP) post-process for performance enhancement. The front end occupies a die area of 1.95 x 1.16 mm$^2$. Its die photograph is shown in Fig. 8.

The whole measurement of the front end was on-wafer performed. The LNA and each SHM draw 17.4 and 3.5 mA from a 1.8-V supply, respectively; therefore, the total current consumption is 24.4 mA. The measured input return loss ($S_{11}$) of the RF front end is shown in Fig. 9. The wideband input impedance matching characteristic ($S_{11}$ below -10 dB from 4.795 to 6.175 GHz) enables the receiver to operate at each frequency band for the WLAN 802.11a standard. The voltage gain of the circuit is measured at different LO power levels as...
shown in Fig. 10. For an LO power below 12 dBm, the voltage gain is more sensitive toward the LO power, where it generally grows by the same amount as the LO power is increased. For an LO power beyond 12 dBm, the voltage gain remains around 24–25 dB no matter how the LO power changes. Therefore, we adopted a 12-dBm LO power to perform all the following measurements. The characteristic of gain versus input frequency is measured as shown in Fig. 11. The voltage gain is increased by 3 dB after the ICP postprocess. Over the 1-GHz frequency band from 4.9 to 5.9 GHz, the front end exhibited a voltage gain larger than 24.5 dB, where a voltage gain of 28.0 dB was achieved at 5.0 GHz. The measured noise figure (NF) with carrier frequency centered at 5.0 GHz is shown in Fig. 12. The spot NF at the 10-MHz baseband is 11.5 and 9.7 dB before and after the ICP postprocess. A stand-alone LNA was also fabricated and measured. At 5 GHz, the measured NF of an LNA is 3.1 dB, and the measured third-order input intercept point (IIP3) is −12 dBm. The two-tone test was performed to characterize the linearity of this circuit. According to the measurement, this receiver front end exhibits an IIP3 of −7.8 dBm and a second-order IIP of 32.8 dBm.

According to the measurement results of gains and NFs, removing the silicon substrate underneath the inductors greatly mitigates the substrate losses seen by the inductors so that a higher gain and a lower NF can be achieved. Another critical effect of removing the silicon substrate underneath the inductors is the improvement in the LO-to-RF isolation. The comparison of the measured LO leakages at the input of the RF front-end chip before and after the ICP postprocess are shown in Fig. 13. It is found that the LO leakage can be effectively reduced by the silicon removal underneath the inductors, and the improvement is 6.8–9.5 dB depending on RF frequencies. According to Fig. 13, the measured LO leakage is below −66 dBm, which means that the achieved LO-to-RF isolation is better than 78 dB over the band of interest. Moreover, the experimental results show that the leakage power grows as the operating frequency is increased, which is probably due to the worse isolation and stronger substrate coupling at higher frequencies.

The LO rejection ratio (LOR) is a primary advantage of the SHM or the receiver adopting SHMs since it contributes to the suppression in the LO self-mixing dc offset. This term is defined as the mixer conversion gain at RF divided by that at the LO frequency [4]. For conventional mixers used in direct downconversion, the amplification or voltage gain for an input RF signal
is identical to that for a signal at LO frequency, and hence, the
LOR is 0 dB. For an SHM, the LOR is theoretically infinite,
which means that the dc offset due to LO self-mixing can be
completely eliminated. However, nonidealities such as layout
mismatches or signal unbalances can lead to considerable degra-
dation in the LOR. As shown in Fig. 14, the measured LOR
is above 35 dB over the band of interest. The dependence of
input-referred dc offset on RF frequency is shown in Fig. 15. It is
found that the LO self-mixing effect is tremendously suppressed
over the band of interest because of the SHM configuration. The
obtained input-referred dc offset due to the LO self-mixing in
this RF front end is $-118.0$ dBm. Since the offset power level
is far below the receiver input noise floor, we may say that the
proposed RF front end is LO self-mixing free.

Lying in the receive band, the 2XLO leakage has the poten-
tial of degrading nearby receivers, which would become an issue
for direct-conversion/low-IF receivers [6]. Therefore, the 2XLO
leakage at the RF port was also measured in order to estimate the
LO reradiation effect. In this work, the measured 2XLO leakage
($-102.7$ dBm at 5.0 GHz) is below the noise floor at the receiver
input ($-101$ dBm considering a 20-MHz bandwidth), and thus,
its reradiation effect is negligible. The performances of the pro-
posed and implemented RF front end are summarized in Table I.

### B. Direct-Conversion Receiver

To demonstrate the proposed receiver architecture, the afore-
mentioned RF front end was further integrated with ABBs and
a fractional-N frequency synthesizer in the CMOS 0.18-μm
process. The die photograph of this fully integrated CMOS
direct-conversion receiver is shown in Fig. 16. The measured
transfer curves of the stand-alone ABB at 5-MHz mode are
shown in Fig. 17, where the 3-dB corner frequencies of the LPF
with and without tuning are 5.004 and 4.2 MHz, respectively.
According to Fig. 17, the accuracy of the LPF is increased
from 84% to 99.92% with the ATL. The measured frequency

### Table I

**Performance Summary of the Proposed Receiver Front-End**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
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</tr>
<tr>
<td>Power Consumption</td>
<td>43.9 mW</td>
</tr>
<tr>
<td>Frequency</td>
<td>5.0 GHz</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>28.0 dB</td>
</tr>
<tr>
<td>NF</td>
<td>9.7 dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>-7.8 dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>+32.8 dBm</td>
</tr>
<tr>
<td>Input-referred DC-offset</td>
<td>-118.0 dBm</td>
</tr>
</tbody>
</table>

Fig. 14. Measured LO rejection of the receiver front end.

Fig. 15. Measured input-referred dc offset of the receiver front end.

Fig. 16. Die photograph of the fully integrated receiver.

Fig. 17. Measured frequency responses with/without ATL at the 5-MHz mode.
responses of the stand-alone ABB at the 5-/10-/20-MHz modes are shown in Fig. 18. Apparently, very precise corner frequencies can be achieved as required due to the ATL function. The measured output spectrum of the stand-alone fractional-N synthesizer is shown in Fig. 19, where the fractional spur at a 4-MHz offset is 74 dBc. The detailed accounts of the performance of this synthesizer are described in [19].

The fully integrated direct-conversion receiver is tested onboard with the on-chip LO generated by its own frequency synthesizer and the ABBs operating at the narrowest bandwidth (5 MHz), middle-gain (40 dB) mode. All control signals are applied through the on-chip TWI circuit. The return losses achieved by five receiver testing boards [printed circuit boards (PCBs)] with series capacitors of 0.47–15 pF are shown in Fig. 20. Note that the on-chip source and gate inductors of the LNA in the RF front end were removed when the RF front end was integrated with the ABBs and the frequency synthesizer. The required inductances are now provided by the gold bonding wires. Due to the bond-wire inductances, the off-chip matching network can be reduced to a surface-mount-device capacitor in series. The effect of bond-wire inductance variation has a huge impact on the input impedance as shown in Fig. 20. For example, PCB 3 and PCB 4 both utilize capacitors of 1.5 pF for input impedance matching but the optimal frequencies of the two PCBs differ by ~250 MHz. The measured frequency response of the fully integrated receiver is shown in Fig. 21 where the receiver exhibits a corner frequency of 5 MHz as expected.

V. SUMMARY

The design of direct-conversion receivers poses a critical challenge in terms of dc offset due to the LO self-mixing. As a solution to this issue, a receiver RF front-end architecture adopting transformer-coupled SHMs and a monolithic quadrature coupler is proposed and fabricated by 0.18-μm CMOS technology in this paper. In addition, the operation principle as well as the advantage of SHMs was introduced. The realized CMOS RF front end demonstrates well-matched input impedance over the band of interest. At 5.0 GHz, the receiver front end exhibits a 28.0-dB voltage gain and a ~7.8-dBm IIP3 while drawing 24.4 mA from a 1.8-V voltage supply. A
fully integrated direct-conversion receiver is also implemented by incorporating the proposed RF front end with ABBs and a frequency synthesizer.

ACKNOWLEDGMENT

The authors would like to thank United Microelectronics Corporation for the chip fabrication and Nano Device Laboratories for the on-wafer measurement assistance.

REFERENCES


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