On-Chip Bidirectional Transceiver

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Abstract—This work presents bidirectional transceiver for on-chip long wires. The current signals are transmitted bidirectionally on the interconnection to double the data rate. The voltage swing on the wire is reduced so that the proposed scheme consumes less power at higher data rate. Using 0.18-µm device models for simulation, the proposed scheme has 1.25-6.80 times of date rate and 37-52% reduction of power/data rate ratio than conventional driver. It also performs higher data rate at an extension of wire length.

I. INTRODUCTION

As the semiconductor process is scaled down, the parasitic effects of interconnections on the very large-scale integrated circuit increase dramatically [1]-[3]. The interconnections are scaled down largely in the horizontal dimension while the vertical dimension is only slightly scaled down. As the width and space of the interconnections decrease, the ratio of wire height to wire width must be increased to prevent the interconnect resistance from increasing greatly. In addition, the totally capacitance, including the bottom capacitance, the adjacent capacitance and the fringing capacitance increase as the wire space decreases. Therefore, the parasitic capacitance and resistance of the interconnections both increase as the process is scaled down.

Replacing the aluminum wire by the copper wire can reduce the parasitic effect. Another scheme is to utilize lower dielectric constant (low-k) as the insulating material. Inserting repeater (buffers) is an efficient solution to reduce the delay on the wires which is commonly used in ICs design [4]-[5]. Besides, reducing the on-wire signal swing is one way to reduce delay and power consumption effectively. However, the reduced signal swing results in insufficient driving capability. It’s usually difficult to operate the circuit in high frequency.

Bidirectional signaling is a popular scheme to double the data rate for chip-to-chip signaling. The precise terminated resistors for chip-to-chip signaling are not suitable for on-chip signaling because of the process variation problem. Moreover, the parasitic wire resistance is proportional to the wire length. The data rate of conventional schemes is severely degraded as the wire length increases. A current-mode bidirectional signaling is becoming important for on-chip long wire transmission [6]-[12].

II. SIMULTANEOUS BIDIRECTIONAL SIGNALING

Fig. 1 shows the conventional bidirectional signaling scheme. A transmitter and a receiver circuity are required to perform the transmitting and receiving of signals, respectively.

Fig. 2 shows the circuitry of the proposed bidirectional current-mode transceiver. The transmitter on the left side consists of transistors P1A, N1A, P2A and N2A. P1A and N1A function as switches at the drain terminals of the current sources P2A and N2A, respectively. Transistors P2A and P3A form a current mirror circuit that transmits the current signal on the wire from P1A to P3A. Transistors N2A and N3A form another current mirror circuit that transmits the current signal on the wire from N1A to N3A. Transistors P3A and N3A and inverter INVA compose the current-compare amplifier converting the current signal to voltage signal. Then the signal is regenerated to full-swing by the output buffer. Transistors P4A (N4A) pulls the node VP1 (VN1) to VDD (GND) when P1A (N1A) is turned off. It guarantees a complete cut-off operation of the current mirror P2A and P3A (N2A and N3A).

Fig. 3 shows the ideal waveforms of the bidirectional signaling scheme. Table I lists the
summary of bidirectional data transmission of two signals.

**Fig. 3. Ideal waveforms of the proposed scheme.**

**Table I Summary of four cases of data transmission.**

<table>
<thead>
<tr>
<th>Case</th>
<th>T1, T2</th>
<th>W1</th>
<th>W2</th>
<th>V1n</th>
<th>V2n</th>
<th>V1o</th>
<th>V2o</th>
<th>V1</th>
<th>V2</th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case1</td>
<td>1</td>
<td>1</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
</tr>
<tr>
<td>Case2</td>
<td>1</td>
<td>0</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
</tr>
<tr>
<td>Case3</td>
<td>0</td>
<td>1</td>
<td>Vt</td>
<td>Vt &lt;Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
</tr>
<tr>
<td>Case4</td>
<td>0</td>
<td>0</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
<td>Vt</td>
</tr>
</tbody>
</table>

**Case 1, (T1, T2) = (1, 1),**

Fig. 4 shows the transmitting and receiving of (T1, T2) = (1, 1). Transistors N1A and N1B are turned on. Transistors P1A and P1B are turned off. Both wire signals W1 and W2 are pulled up to Vtn. There is no current path on transistors N1A and N1B. Transistors P3A and N3A are turned off.

The formula of signal voltages on the wire for the case (T1, T2) = (1, 1) are as following,

\[ V_{W1} = V_{DS,N1A} + V_{GS,N1A} = V_{tn} \]  
\[ V_{W2} = V_{DS,N1B} + V_{GS,N1B} = V_{tn} \]

The NMOS device of INVA is cut-off and the output of INVA is charged by PMOS current IP to logic 1.

**Case 2, (T1, T2) = (1, 0),**

Fig. 5 shows the transmitting and receiving of (T1, T2) = (1, 0). Transistors N1A and P1B are turned on. Transistors P1A and N1B are turned off. The wire signal W1 is pulled to V1-0, which is larger than Vtn. The wire signal W2 is pulled to V0-1 which is lower than VDD-|V_{tp}|. There is a current path through transistors N1A and P1B.

The formula of signal voltages on the wire for the case (T1, T2) = (1, 0) are as following,

\[ V_{W1} = V_{DS,P1B} + IR + V_{DS,N1A} + V_{GS,N1A} = V_{DD} \]  
\[ V_{W2} = V_{PN} = V_{DD} - \frac{2I}{V_{W(L)P2B}} \]  
\[ V_{W1} = V_{PN} = \frac{2I}{V_{W(L)N2B}} + V_{tn} + V_{DS,N1A} \]

The voltage difference on the two ends of the wire is,

\[ V_{W2} - V_{W1} = V_{1-0} - V_{0-1} = IR \]  
\[ V_{PN} = V_{DD} - \frac{2I}{V_{W(L)P2B}} - \frac{V_{W(L)P2B}}{V_{W(L)N2B}} \]

The devices can be sizing to enlarge (W/L)_{P2B} and (W/L)_{N2A} and minimize V_{SD,P1B} and V_{DS,N1A} to obtain the largest signal swing (V_{W2}-V_{W1}) of the wire.

The analysis of signal receiving on the left side is described as following. P3 A is cut-off. The output PMOS current and NMOS current of INVA are IP and IN, respectively. Assume V_{DS,N1A} ≈ 0. Then V_{DS,N1A} ≈ V_{GS,N1A} ≈ V_{1-0}. The equations of the current can be formula as,

\[ I_p = \frac{1}{2} k_p (\frac{W}{L})_p (V_{GS,p} - |V_p|)^2 \]  
\[ I_n = \frac{1}{2} k_n (\frac{W}{L})_n (V_{GS,n} - |V_n|)^2 \]  
\[ I_{n3a} = \frac{1}{2} k_n (\frac{W}{L})_{n3a} (V_{GS,n3a} - |V_n|)^2 \]  
\[ I_{n3b} = \frac{1}{2} k_n (\frac{W}{L})_{n3b} (V_{n3b} - |V_n|)^2 \]

If (W/L)_{n3a}=(W/L)_{n}, providing I_{n3a}=I_n. At the output of INVA, the total discharging current is (I_{n3a} + I_n)=2I_n. Since V_{1-0} is less than 1/2V_{DD}, I_n < I_p. The discharging and charging current at the INVA output are compared to obtain the receiving signal. The following condition maintains logic 0 at the INVA output,

\[ 2I_n > I_p \]

The receiving signal R2 obtains logic 0 after a
non-inverting buffer.

The analysis of signal receiving on the right side is as following. N3B is cut-off. Assume $V_{DS,P1B} \approx 0$. Then $V_{GS,P3B} \approx V_{GS,P2B} \equiv V_{0,1}$. The equations of the current can be formula as,

$$I_p = \frac{1}{2} k_p \frac{W}{L} (V_{GS,P1} - |V_p|)^2$$

$$I_n = \frac{1}{2} k_n \frac{W}{L} (V_{GS,N1} - |V_n|)^2$$

$$I_{P1A} = \frac{1}{2} k_p \frac{W}{L} (V_{GS,P1A} - |V_p|)^2$$

$$I_{P3B} = \frac{1}{2} k_p \frac{W}{L} (V_{0,1} - |V_p|)^2$$

If $(W/L)_{P3A} = (W/L)_{P}$, providing $I_{P3A} = I_P$. At the output of INVA, the total charging current is $(I_{P1A} + I_N) = 2I_P$. Since $V_{0,1}$ is larger than $1/2V_{DD}$, $I_P < I_N$. The discharging and charging current at the INVA output are obtained to receive the signal. The following condition maintains logic 1 at the INVA output,

$$2I_P > I_N$$

(15)

The receiving signal R1 obtains logic 1 after a non-inverting buffer.

**Case 3, (T1, T2) = (0, 1),**

Fig. 6 shows the transmitting and receiving of (T1, T2) = (0, 1). Transistors P1A and N1B are turned on. Transistors N1A and P1B are turned off. The wire signal $W1$ is pulled to $V_{0,1}$ which is lower than $V_{DD} - |V_{tp}|$. The wire signal $W2$ is pulled to $V_{1,0}$ which is larger than $V_{tn}$. There is a current path through transistors P1A and N1B. The formula analysis of transmitting and receiving of bidirectional signals are similar to the description of case 3 in Eqs. (4)-(15). As a result, R1 and R2 receive logic 0 and logic 1, respectively.

**Case 4, (T1, T2) = (0, 0),**

Fig. 7 shows the transmitting and receiving of (T1, T2) = (0, 0). Transistors P1A and P1B are turned on. Transistors N1A and N1B are turned off. Both wire signals $W1$ and $W2$ are pulled up to $V_{DD} - |V_{tp}|$. There is no current path on transistors P1A and P1B. Transistors P3B and N3B are turned off.

**III. SIMULATIONS AND COMPARISONS**

The 0.18-um single-poly six-metal CMOS process device models are used for simulation. For minimum width and space of metal one, the unit parasitic resistance and capacitance are 339 mΩ and 0.246 fF, respectively. The 3π segment model shown in Fig. 8 is used for wire simulation.
Fig. 8. 3π segment model of wire.

Fig. 9 compares the maximum data rate on various wire lengths. It is seen this work performs higher data rate. Fig. 10 demonstrates that this work has smaller ratios of power/data rate. As the wire length is increased, the speedup is enhanced and the ratio of power to data rate is reduced. The proposed transmitter shows better potential for long wire transmission at an extension of wire length in the deep submicron process. Fig. 11 displays the chip photograph of the transceiver.

IV. CONCLUSION

A simultaneous bidirectional signaling scheme is presented in this work. The circuitry performs simultaneous bidirectional transmission using current-mode signal. The voltage swing on the wire is reduced so that the proposed scheme consumes lower power and obtains higher data rate. Simulation using 0.18-µm SPICE model shows that the proposed transmitter has 1.25-6.80 times of maximum data rate and 37-52% reduction of power/data rate ratio.

V. REFERENCES