A Basic Study on a Very Low-Level DC Current Amplifier Using a Switched-Capacitor Circuit

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SUMMARY In order to miniaturize a very low-level dc current amplifier and to speed up its output response speed, we proposed to employ the switched-capacitor circuit (SCC) as its negative feedback circuit, instead of the conventionally used high-ohmage resistor. However, in the case of using SCC, the output waveform had unnecessary components. To decrease the effect of these components and to speed up the response speed, we used a switched-capacitor filter (SCF), an offset controller, and a positive feedback circuit. As a result, we demonstrated that it was useful to use the amplifier using the SCC.

key words: dc amplifier, small current measurement, negative feedback, positive feedback, switched-capacitor

1. Introduction

When very small ion currents are measured by mass spectrometers and radiation detectors, the response speeds of the measuring instruments are limited by those of very low-level dc current amplifiers [1]–[3]. This means that these amplifiers are required to observe rapid transient phenomena. In general, the very low-level dc current amplifier for measuring small currents is composed of an amplifier that has high-input impedance and a high-ohmage resistor as its negative feedback circuit. In the output of this amplifier, a voltage drop is produced by an unknown small current flowing through the high-ohmage resistor of a known value. Thus, we can obtain the value of the small current by Ohm’s law [1]–[3]. An amplifier using a high-ohmage resistor is not appropriate for miniaturization and has undesirable and unavoidable effects of the stray capacitances across its terminals. The latter factors especially cause the amplifier to have complicated frequency characteristics, which results in the poor responses of the very low-level dc current amplifier [4], [5]. In order to decrease its effective input capacitance and to speed up its output response speed, a positive feedback circuit had been employed [4], [5]. In this case, however, the amplifier was unstable and began to oscillate. As a result, high speed response of the amplifier could not be obtained.

Therefore, to improve the above problems, we proposed to employ the switched-capacitor circuit (SCC) in the negative feedback circuit. The SCC is equivalent to a resistor and is suitable for miniaturization. And transient phenomena of the output waveforms of the very low-level dc current amplifier were investigated by means of computer simulation [6], [7]. However, vibrations and offset components in the output voltage were generated by charge and discharge actions of the SCC and clock feed through (CFT) of analog switches. In this paper, we investigated the elimination of these unnecessary components of the amplifier using an SCC with a switched-capacitor filter (SCF) and an offset controller. Furthermore, the positive feedback circuit was also used to speed up the response speed [8].

2. Circuit Description

The very low-level dc current amplifier using SCC, including the positive feedback circuit, SCF, and a small current source, is shown in Fig. 1. The symbols used for the amplifier are as follows. $K$ is amplification of the amplifier having a high-input resistance and $C_p$ and $R_p$ are the input capacitance and input resistance, respectively. In the experiment, we utilized a triangular-wave voltage produced by the function generator and the differentiating capacitor $C_S$ (re-actance attenuator) to obtain a square-wave current $I_S$ having high-output impedance as the input signal to the amplifier. $C_D$ is the output capacitance to the ground of $C_S$. The positive feedback circuit is composed of a positive feedback capacitance $C_f$ and a positive feedback amplification $K_f$. The negative feedback circuit is comprised of an SCC and a feedback rate attenuator, which is able to increase the amplification of the amplifier. As a result, using the feedback rate attenuator reduces the Miller effect. The SCC is composed of four analog switches ($S_1$, $S_2$, $S_3$, and $S_4$) and a capacitor $C_1$. It is assumed that $S_1$ and $S_3$ are synchronous with $S_2$ and $S_4$, respectively, and that the four switches are controlled by two non-overlapping clock signals. Therefore,
the equivalent resistance \( R_{SC} \) of the SCC is determined by the values of \( C_1 \) and the clock frequency \( f_s \) \((R_{SC} = 1/C_1 f_s)\) [9].

3. Circuit Analysis

In this section, we analyzed the output response speed, the theoretical output voltage of the very low-level dc current amplifier, and the principle of operation of the SCF.

3.1 Output Resonse Characteristic of the Very Low-Level dc Current Amplifier

An input equivalent circuit of the very low-level dc current amplifier using the SCC is shown in Fig. 2(a). In this case, we assume that a small current \( I_s \) is dc current because the clock frequency \( f_s \) of the SCC is much higher than the frequency of \( I_s \). We further assume that \( T_1 \) is the time when \( S_1 \) and \( S_2 \) are closed \((S_1 \) and \( S_2 \) are opened), and \( T_2 \) is the time when \( S_1 \) and \( S_2 \) are opened \((S_1 \) and \( S_2 \) are closed).

The voltage \( V_z \) at the node \( z \) in Fig. 2(a) is given by

\[
V_z = \frac{R_1}{R_1 + R_2} (-KV_1).
\]

Thus, Millman’s theorem is applied to Fig. 2(a), and the voltage \( V_1 \) is represented by

\[
V_1 = \frac{j\omega C_1 K_1 + j\omega C_1 (-KV_1) + I_s}{\frac{1}{R_g} + j\omega (C_1 + C_2 + C_p + C)}.
\]

where \( \omega \) is the angular frequency, \( C \) is capacitance in the negative feedback circuit and is given by

\[
C = \begin{cases} 
C_1 + C_{\alpha} & (T_1: \ S_1 \ and \ S_2 \ are \ closed) \\
\alpha C_{\alpha} & (T_2: \ S_3 \ and \ S_4 \ are \ closed),
\end{cases}
\]

where \( \alpha \) is parasitic capacitance component of the analog switches. Therefore, input admittance of the amplifier, \( Y_{in} \), is given by

\[
Y_{in} = \frac{I_s}{V_1} = \frac{1}{R_g} + j\omega \left[ C_1 + C_{\alpha} + (1 - K_p)C_g + \left(1 + \frac{R_1}{R_1 + R_2}K\right)C_{\alpha}\right].
\]

In fact, a clock feed through is caused by the parasitic capacitance \( C_{\alpha} \) across its terminals for simplicity of the circuit analysis. In depth investigation with respect to the clock feed through will be discussed in a future paper.

The effective input resistance, \( R_{in} \), and the effective input capacitance, \( C_{in} \), are given as follows:

\[
R_{in} = R_g,
\]

and

\[
C_{in} = C_1 + C_{\alpha} + (1 - K_p)C_g + \left(1 + \frac{R_1}{R_1 + R_2}K\right)C_{\alpha}.
\]

The simplified input equivalent circuit of the very low-level dc current amplifier using the SCC is shown in Fig. 2(b). For simplicity, \( C_1 \) and \( R_{SC} \) of the SCC are converted into \( C'_1 \) and \( R'_{SC} \) in the equivalent circuit at the input of the amplifier, respectively. In this case, \( C'_1 \) is given by

\[
C'_1 = \left(1 + \frac{R_1}{R_1 + R_2}K\right)C_1.
\]

Further, \( C'_1 \) is alternately connected to the left-hand side of the circuit and GND. The equivalent resistance \( R'_{SC} \) is given by

\[
R'_{SC} = \frac{1}{R_{SC} f_s} = \frac{R_{SC}}{1 + \frac{R_1}{R_1 + R_2}K}, \tag{1}
\]

where \( f_s \) is the clock frequency. Therefore, the input admittance \( Y_{in} \) in Fig. 2(b) is represented by

\[
Y_{in} = \frac{1}{R_g} + \frac{1}{R_{SC} f_s} + j\omega \left[ C_1 + C_{\alpha} + (1 - K_p)C_g + \left(1 + \frac{R_1}{R_1 + R_2}K\right)C_{\alpha}\right]. \tag{2}
\]

From Eq. (2) and \( R_g \gg R'_{SC} \), the time constant of the amplifier, \( \tau_{in} \), is given as follows:

\[
\tau_{in} = \frac{1}{R_g} + \frac{1}{R_{SC} f_s} \left[ C_1 + C_{\alpha} + (1 - K_p)C_g + \left(1 + \frac{R_1}{R_1 + R_2}K\right)C_{\alpha}\right] \\
\approx R'_{SC} \left[ C_1 + C_{\alpha} + (1 - K_p)C_g + \left(1 + \frac{R_1}{R_1 + R_2}K\right)C_{\alpha}\right]. \tag{3}
\]
From Eqs. (2) and (3), we can see that the Miller effect reduces by using the feedback rate attenuator because the value of \( R_1 / (R_1 + R_2) \) is smaller than unity \( (R_1 / (R_1 + R_2) < 1) \), and that the effective input capacitance is decreased by using the positive feedback circuit because the positive feedback capacitance \( C_p \) acts as a negative capacitance when \( K_p > 1 \).

### 3.2 Theoretical Output Voltage

The output voltage of the very low-level dc current amplifier has vibrations and an offset voltage due to charge and discharge actions of the SCC and the CFT. The enlarged output voltage waveform of the amplifier at a positive final steady-state is shown in Fig. 3.

Let the switching period of the switches be \( T_S \) and the output voltage of the amplifier at \( t = nT_S \) be \( V_0(n) \). Subscript symbols ‘+’ and ‘−’ mean just after and just before the time event occurs, respectively. For example, \( V_0(n+1)_- \) means the voltage just before \( t = (n + 1)T_S \). Assume that rapid changes in the output voltage from \( T_2 \) to \( T_1 \) is \( V_1 \) and those from \( T_1 \) to \( T_2 \) is \( V_2 \). The output voltages at each time are

\[
V_0(n)_- = V_0\left(n - \frac{1}{2}\right)_- + \frac{1}{C_a} \int_{(n-\frac{1}{2})T_S}^{nT_S} i_1 \, dt \\
= V_0\left(n - \frac{1}{2}\right)_- + \frac{i_S T_S}{2C_a},
\]

\[
V_0\left(n + \frac{1}{2}\right)_+ = V_0\left(n + \frac{1}{2}\right)_- - V_2, \tag{4}
\]

\[
V_0(n + 1)_- = V_0(n)_+ + \frac{1}{C_1 + C_a} \int_{nT_S}^{(n+\frac{1}{2})T_S} i_1 \, dt \\
- V_2 + \frac{i_S T_S}{2C_a} \\
= V_0(n)_+ + \frac{i_S T_S}{C_1 + C_a} - V_2 + \frac{i_S T_S}{2C_a}. \tag{5}
\]

The term \( V_0(n + 1/2)_- \) of Eq. (5) represents the peak voltage during \( T_1 \). Additionally, electric charges of the SCC are conserved just before and after \( t = nT_S \). We obtain

\[
V_0(n)_- = \frac{C_1 + C_a}{C_a} V_0(n)_+ . \tag{7}
\]

Since \( V_0(n)_- = V_0(n + 1)_- \), from Eqs. (4) and (6) we obtain

\[
V_0\left(n - \frac{1}{2}\right)_+ = V_0(n)_+ + \frac{1}{C_1 + C_a} \frac{i_S T_S}{2} - V_2. \tag{8}
\]

Further \( V_0(n - 1/2)_+ = V_0(n + 1/2)_+ \); hence, from Eqs. (5) and (8) we obtain

\[
V_0\left(n + \frac{1}{2}\right)_+ = V_0(n)_+ + \frac{1}{C_1 + C_a} \frac{i_S T_S}{2}. \tag{9}
\]

In addition, since \( V_0(n)_- = V_0(n + 1)_- \), from Eqs. (6) and (7) we obtain

\[
V_0(n)_+ = \frac{C_a}{C_1 + C_a} \frac{i_S T_S}{2} - \frac{C_a}{C_1} V_2 + \frac{i_S T_S}{2C_1}. \tag{10}
\]

Substituting Eq. (10) into Eq. (9) gives the peak voltage during \( T_1 \):

\[
V_0\left(n + \frac{1}{2}\right)_+ = \frac{i_S T_S}{C_1} - \frac{C_a}{C_1} V_2 \\
= \frac{i_S R_{SC}}{C_1} - \frac{C_a}{C_1} V_2. \tag{11}
\]

From Eq. (11), we can understand that the peak voltage during \( T_1 \) includes the theoretical voltage \( (i_S R_{SC}) \) and the offset voltage \( (C_a V_2) \). Therefore, the theoretical output voltage can be obtained by sampling the peak voltage during \( T_1 \) using the SCF and by cancelling out the offset voltage using the offset controller.

### 3.3 The Principle of Operation of the SCF

As stated above, the output voltage of the very low-level dc current amplifier has vibrations due to charge and discharge actions of the SCC. Therefore, we must sample the peak voltage during \( T_1 \). In our research, we proposed to use the SCF not as a low-pass filter but as a sample-and-hold circuit to obtain the peak voltage during \( T_1 \). The circuit configuration of the SCF is shown in Fig. 1.

Switches \( S_5 \) and \( S_6 \) are synchronous with \( S_1 \) (\( S_2 \)) and \( S_3 \) (\( S_4 \)), respectively. Therefore, the peak voltage during \( T_1 \), which is the theoretical voltage \( (i_S R_{SC}) \), is charged by the capacitor \( C_i \). In the next period \( T_2 \), the electric charge at \( C_i \) is discharged and transferred to \( C_0 \). When the action is repeated, the output voltage \( V_{O2} \) equals the input voltage \( V_O \). The operating state of the SCF is shown in Fig. 4.

Firstly, it is assumed that the ON resistances of the \( S_5 \) and \( S_6 \) are \( R_S \) and \( R_6 \), respectively, and that the OFF resistances of these switches are infinite. From Fig. 4(a), when \( S_5 \) is closed at \( t = nT_S \), we obtain the differential equation as follows:

\[
\frac{dq_{n}(t)}{dt} + \frac{q_{n}(t)}{R_S C_i} = \frac{V_O}{R_S} \tag{12}
\]
where \( nT_{S_+} \leq t_1 \leq (n + 1)/2T_{S_+} \). Since the electric charge \( q_{ct} \) at \( C_t \) does not change just before and after \( t = nT_S \), the initial condition \( q_{ct}(n)_+ \) is given by

\[
q_{ct}(n)_+ = q_{ct}(n)_-,
\]

if we consider \( t_1 = nT_{S_+} \) as the initial time during \( T_1 \). Therefore, the general solution of Eq. (12) is represented by

\[
V_{ct}(t_1) = V_{ct}(n)_- \exp \left( -\frac{t_1 - T}{\tau_1} \right) + V_O \left[ 1 - \exp \left( -\frac{t_1 - T}{\tau_1} \right) \right],
\]

where the time constant \( \tau_1 = R_SC_t \) and \( T = nT_{S_+} \). From Eq. (13), \( V_{ct}(t_1) \) equals \( V_O \) at a steady-state. Furthermore, \( V_O \) equals the peak output voltage of the amplifier during \( T_1 \) because \( S_S \) is closed during \( T_1 \). From Fig. 4(a), it is clear that the output voltage \( V_{ch}(t_1) = V_{ch}(t_0) \) is constant during \( T_1 \).

Secondly, from Fig. 4(b), when \( S_S \) is closed at \( t = (n + 1/2)T_S \), we obtain the differential equations during \( T_2 \) as follows:

\[
V_{ct}(t_2) = \frac{R_SC_h}{C_t} \frac{dV_{ch}(t_2)}{dt} - V_{ch}(t_2) = 0,
\]

and

\[
C_t \frac{dV_{ct}(t_2)}{dt} + C_h \frac{dV_{ch}(t_2)}{dt} = 0,
\]

where \( (n + 1/2)T_{S_+} \leq t_2 \leq (n + 1)T_{S_+} \). Integrating Eq. (14) from \( (n + 1/2)T_{S_+} \) to \( t_2 \) gives

\[
V_{ct}(t_2) = V_{ct}(n + 1/2)_+ + \frac{C_h}{C_t} V_{ch}(n + 1/2)_- - \frac{C_h}{C_t} V_{ch}(t_2).
\]

Since voltages \( V_{ct} \) and \( V_{ch} \) do not change just before and after \( t = nT_S \), the initial conditions \( V_{ct}(n + 1/2) \), and \( V_{ch}(n + 1/2)_+ \) are given by

\[
V_{ct}(n + 1/2)_+ = V_{ct}(n + 1/2)_- = V_O,
\]

and

\[
V_{ch}(n + 1/2)_+ = V_{ch}(n + 1/2)_-,
\]

respectively, if we consider \( t_2 = (n + 1/2)T_{S_+} \) as the initial time during \( T_2 \). Substituting Eq. (16) into Eq. (14) gives the following differential equation:

\[
\frac{dV_{ch}(t_2)}{dt} + \left( \frac{C_t + C_h}{R_SC_t} \right) V_{ch}(t_2) = \frac{V_O}{R_SC_h} + \frac{V_{ch}(n + 1/2)_-}{R_SC_t}.
\]

(17)

The general solution of Eq. (17) is represented by

\[
V_{ch}(t_2) = \frac{C_t}{C_t + C_h} \left[ 1 - \exp \left( -\frac{t_2 - T'}{\tau_2} \right) \right] V_O + \frac{C_h}{C_t + C_h} \left[ 1 + \frac{C_t}{C_h} \exp \left( -\frac{t_2 - T'}{\tau_2} \right) \right] V_{ch}(t_1).
\]

(18)

From Eq. (19), we can understand that when the charge and discharge actions are repeated, \( V'_O \) equals \( V_O \). For example, in the case \( C_t = C_h \), the relationship between \( V'_O \) and \( V_O \) are expressed as

\[
V'_O = \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \cdots \right) V_O.
\]

From the above results, we can understand that the SCF acts as a sample-and-hold circuit. Note that using a sample-and-hold circuit generally requires a clock generator that completely differs from two non-overlapping clock signals utilized by the SCC. On the other hand, using the SCF allows for sharing the two non-overlapping clock signals. Therefore, the SCF is useful from the viewpoint of miniaturization.

4. Experimental Results

The very low-level dc current amplifier using SCC as shown in Fig. 1 was made. The amplification \( K \) of the amplifier having high-input impedance was 62 dB (DC ~ 1.2 MHz), and output voltage waveforms were observed using an oscilloscope. Since the triangular-wave voltage, which had a time period of 5 ms and an amplitude of 10 V, was differentiated by the differentiating capacitor \( C_s \) (1.25 pF), a square-wave having a time period of 5 ms and an amplitude of 10 nA was obtained as an input current \( I_2 \) to the amplifier. The equivalent resistance \( R_{SC} \) of the SCC was set to 1 MΩ.
by using a styrol capacitor $C_1$ of 10.3 pF and by adjusting the value of the clock frequency $f_S$. The attenuation $X$ of the feedback rate attenuator, consisting of $R_1$ of 96.0 $\Omega$ and $R_2$ of 10.3 k$\Omega$, was set to 1/100. As a result, the total equivalent resistance $R_f (= R_{SC}/X)$ of the negative feedback circuit was set to 100 M$\Omega$. We used C-MOS analog switches (MAX326, MAXIM Integrated Products, Inc.), the maximum leakage current of which was 10 pA, as switches of the SCC. The value of $C_p$ was set to 2 pF.

An SCF and an offset voltage controller, which were connected to the input of the amplifier and had a gain of unity, were also used in this experiment. The input stage of the offset controller was composed of a J-FET which had higher input impedance than the negative feedback circuit, and its voltage drift was very small (several $\mu$V). Therefore, the offset controller did not have much effect on the current detection sensitivity of the amplifier.

4.1 Without the Positive Feedback Circuit

Figures 5(a) and 5(b) show the output voltage waveform of the very low-level dc current amplifier and its enlarged waveform at a positive final steady-state in the case without $K_p$. In this case, peak values of the output voltage during a period $T_1$ became 1 V by using the clock frequency $f_S$ of 74.1 kHz; however, the theoretical value was 97.1 kHz. The offset voltage was adjusted by the offset controller until the theoretical output voltage, which was observed during the time period $T_1$, was centered at GND level to obtain its symmetric amplitude.

From Figs. 5(a) and 5(b), we found the output voltage of the very low-level dc current amplifier had vibrations due to charge and discharge actions of the SCC as mentioned in Section 3. Parasitic capacitances in the terminals between drain-source, gate-drain, and gate-source in the C-MOS switches caused the output waveform of the amplifier to have a margin of error.

Peak values of the output voltage during $T_1$ were sampled by the SCF. The result is shown in Fig. 5(c). The output voltage $V'_O$ of the SCF has the offset voltage due to the CFT. In the following experiments, we adjusted the offset voltage until $V'_O$ was centered at GND level by using the offset controller. From Fig. 5(c), it is clear that using the SCF drastically reduces vibrations as well as unnecessary components, and that the input current $I_S$ is obtained by measuring the amplitude value of its output voltage. With respect to the Fig. 5(c), the rise time $t_r$ of the output waveform of the SCF is 36.4 $\mu$s. The rise time, here, is the time required for the output waveform to rise from 10% to 90% of its final steady-state value, as defined in general. The output waveform of the very low-level dc current amplifier using the high-ohmage resistor without $K_p$ is shown in Fig. 6. In this case, the rise time is 83.8 $\mu$s.

4.2 With the Positive Feedback Circuit

Figures 7(a) and 7(b) show the output voltage waveform of the very low-level dc current amplifier and its enlarged waveform at a positive final steady-state in the case with $K_p$. Comparing Figs. 5(a) and 5(b) to Figs. 7(a) and 7(b), respectively, we found that the vibration width of the output voltage increased in the case with the positive feedback circuit.

Peak values of the output voltage during the period $T_1$ were sampled by the SCF. The result is shown in Fig. 7(c). From Fig. 7(c), we could obtain the output voltage having
Table 1  The relationship between rise time $t_r$ and $K_p$.

<table>
<thead>
<tr>
<th></th>
<th>Without $K_p$</th>
<th>With $K_p$</th>
</tr>
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<tbody>
<tr>
<td>High-ohmage resistor</td>
<td>83.8 µs</td>
<td>62.3 µs</td>
</tr>
<tr>
<td>SCC</td>
<td>36.4 µs</td>
<td>24.0 µs</td>
</tr>
</tbody>
</table>

Table 1 shows the relationship between rise time $t_r$ and $K_p$, in both the cases using the high-ohmage resistor negative feedback circuit and using the SCC. It was clear from Table 1 that the response of the very low-level dc current amplifier using the SCC was better than that of the amplifier using the high-ohmage resistor from the viewpoint of speeding up its response speed. Therefore, using the SCC with a positive feedback circuit is an effective way to obtain faster performance of the very low-level dc current amplifier. Moreover, using the SCC and the SCF significantly led to the improvement of the signal to noise ratio, as compared to the case of using a high-ohmage resistor with the positive feedback circuit.

5. Conclusion

In this paper, we demonstrated that a small current of 10 nA could be measured by a very low-level dc current amplifier using an SCC and an SCF, and that it was useful to include the positive feedback circuit from the viewpoint of speeding up its response speed. A circuit configuration of SCC and SCF, which do not have much effect on the clock feed through, will be considered as the next step of our research.

References

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