We present a comprehensive review of product level reliability challenges for the 65nm technology node. The major reliability degradation mechanisms are analyzed for CMOS technologies. Historical data will show that hot carrier degradation has lost on importance and that negative bias temperature instability (NBTI) is the leading reliability concern for the 65nm technology node. Additionally, dielectric breakdown as well as gate leakage currents pose an important limitation to the maximum applicable voltage across the gate oxide. Product standby currents and regulator design are highly influenced by transistor reliability. We will present product reliability data ensuring sufficient product level reliability as well as their correlation attempts to transistor level data.

Introduction

The gate dielectric has been the subject of constant improvement and innovation since the invention of the MOSFET transistor. The gate oxide is the major transistor component to control the transistor channel underneath with respect to leakage currents as well as saturation drive currents. The demand for higher drive currents and better performance has also pushed the gate oxide thickness towards its material limits, especially as we enter the 65nm technology node. The common candidate for the ultimate gate dielectric, silicon dioxide, is facing its structural boundaries and silicon dioxide/nitride stacks will become mainstream for 65nm technologies and beyond. The medium dielectric k-number of nitride allows thicker physical oxides to control direct tunneling currents. However, the ultimate dielectrics are high k-number gate materials such as hafnium oxide or zirconium oxide. Both dielectric materials have still not demonstrated comparable carrier mobilities as well as dielectric integrity and reliability. In addition, high-k dielectrics suffer from severe charge trapping effects reducing the reliability drastically as well as new breakdown phenomena never experienced before with silicon dioxide based gate oxides[1][2].

We will focus on nitrided gate oxides in this presentation and discuss the different reliability concerns. As drive currents increase HCI reliability usually gets worse since the drive current directly determines the carriers generated by impact ionization. Lightly-doped drain (LDD) optimization, however, reduces the electric field at the drain edge significantly. Overall the substrate current, which is a quantitative measure for impact ionization, is strongly reduced for advanced CMOS technologies. Figure 1 gives the minimum and maximum substrate current for technology nodes starting form the last decade. The maximum substrate current considers the worst case poly CD variation for the given technology node.
FIGURE 1: DEVELOPMENT OF NOMINAL AND MAXIMUM SUBSTRATE CURRENT (IBB) FOR DIFFERENT TECHNOLOGY NODES. THERE IS A CLEAR TREND OF DECREASING IBB WITH MORE ADVANCED DEEP SUB-MICRON TECHNOLOGIES.

Generally HCI reliability is only an issue for NMOS transistors, since Arsenic is used as the most common LDD dopant. Due to the low diffusivity of Arsenic steep doping junctions can be manufactured causing higher fields at the drain gate edge compared to PMOS LDD regions, where mostly Boron is employed as LDD dopant. Since Boron exhibits excessive diffusion several techniques have to be applied to control the effective gate length, such as offset spacers or low thermal budget processing. The high diffusivity causes LDD junction to be less steep and hence a lower electric field at the LDD edge. Generally, HCI reliability tests are conducted at room temperature because elevated temperatures would cause a mobility reduction, which on the other hand reduces the drive current and reduces the generated hot carriers. Historically, the maximum substrate current was found at about Vcc/2 and further increase in gate bias reduced the substrate current due to a lower gate-to-drain field. Since the 90nm technology node the gate bias for the maximum hot carrier stress has shift to full Vcc or beyond due to the fact that the lateral field becomes dominant. The shift in worst case HCI biasing is not observed for thick gate oxide devices, e.g. I/O transistors, because those transistors cannot be scaled aggressively due to the high external bias conditions (2.5-3.3V). Therefore, I/O transistors may suffer severe HCI degradation when the drain field is not optimized correctly. Summarizing, HCI is not a reliability concern for deep sub-micron transistors below the 90nm technology. However, I/O transistors still need to be carefully monitored and optimized for HCI reliability. As an alternative to eliminate I/O transistors advanced circuit techniques can be applied to avoid dual or triple gate oxide technologies [3].

The second considerable reliability concern is time dependent dielectric breakdown (TDDB). The TDDB lifetime is usually measured in the weak inversion regime. Generally, the lifetime is strongly dependent on the maximum junction temperature, the applied maximum gate voltage and the stressed gate oxide area. The maximum applied gate voltage in a circuit is mostly limited by the gate induced leakage current (GIDL) for low power products which can be the major off-state leakage current component. For high speed 65nm technology products the maximum gate bias is chosen to meet the
performance requirements. TDDB can be mostly improved by lowering the gate stress or by understanding the circuit behavior of the critical transistors in more detail. The TDDB lifetime significantly improves if AC signals are applied to the stressed transistor compared to a constant DC stress. Generally, TDDB lifetime improves for a higher nitrogen concentration in the gate oxide, but it also cause more positive charges being created during NBTI stressing [4]. The biggest concern with regards to TDDB reliability results from the recent trend of over driving the transistors with higher gate voltages to improve the saturation currents. The gate overdrive cause a significant impact on the gate oxide reliability and does not improve the fundamental CV/I performance metrics. This trend has been recognized in the recent ITRS roadmap, where the supply voltages have been adjusted to higher values reflecting the urge for higher drive currents[5]. Oghata et al. [6] have given the time to breakdown for different gate oxides over a wide range of stress voltages (see Figure 2). A very consistent trend is found for the power law exponent for NMOS and PMOS transistors justifying the use of the power law voltage dependence to evaluate dielectric breakdown for ultrathin gate oxides (<35Å). Historically, the E-model or 1/E models were used to model the dielectric breakdown voltage dependence.

![Normalised Time to Breakdown for Different Gate Oxides](image1)

**FIGURE 2:** TIME TO DIELECTRIC BREAKDOWN FOR DIFFERENT ULTRATHIN GATE OXIDES USING THE POWER LAW. POWER LAW EXPONENTS ARE FOUND TO VARY BETWEEN 33-45 FOR NMOS AND PMOS DEVICES FROM [6].

In contrary to HCI degradation TDDB shows a strong temperature dependence and degrades with elevated temperatures. Since the drive currents degrade at higher temperatures – mobility reduction – the hot carrier generation rate also degrades leading to higher HCI lifetimes. For TDDB the lifetime degrades significantly due to the increase of the bulk trap generation rates leading to percolation currents in the gate oxides [7]. For practical purposes the TDDB lifetime depends significantly on the detection of the onset of soft breakdown vs. hard breakdown. Different soft breakdown models have been discussed in the literature, however, engineering judgment is still used to determine the exact soft breakdown event.
I. NBTI Reliability

Since the introduction of heavily nitrided gate oxides the NBTI phenomena gained significantly on importance. Significant work has been published on the NBTI reliability for standard DC test conditions ($V_s, V_d, V_b=0.0V$) as well as under pulsed conditions[8-11]. The relaxation phenomena was deeply investigated and characterized. We will present experimental data which clearly show the impact of the measurement equipment as well as relaxation time between stress cycles on the overall NBTI reliability. However, the role of hydrogen is still not fully understood [11]. Less work was published on the circuit level reliability degradation due to NBTI and the impact of relaxation. This work is analyzing all possible circuit level biasing conditions, maximum operating temperatures, and operating cycles to understand the impact on the circuit level. A simple analytical reliability model is referenced to estimate the threshold voltage shift during real operation conditions. This additional threshold voltage shift is counting against the design margin budget and, hence, has to be added to the SS corner at elevated temperature in order to evaluate the worst case circuit conditions.

In the following sections we will focus on three levels of investigations: the transistor level, the ring oscillator level (RO) and the product level. It will be shown that each of this reliability levels will have significantly different results with respect to NBTI lifetimes demonstrating that NBTI is a very complex phenomena which might be very difficult to link from transistor level to product level. Historically that is a huge paradigm shift for reliability engineering since the other two reliability components (HCI and TDDB) can still be estimated on a product level by analyzing the transistor level data.

II. Transistor Level Reliability

Numerous transistor level reliability data and degradation curves have been published in the recent literature on NBTI. It can be noted that mostly either saturation drive current, threshold voltage or linear current degradation is reported. Since those quantities are fundamentally connected they can be correlated easily. A typical threshold degradation plot for a 90nm PMOS transistor is shown in Figure 3.

**Figure 3:** Stress plot for extrapolation of NBTI lifetime for a 10/10 90nm PMOSFET device. The lifetime can be extrapolated for different $V_{TSAT}$ criteria.
The degradation plot shows basically two degradation slopes and allows the calculation of the 10% degradation lifetime through extrapolation. The degradation was measured using a probe station employing a S-M-S (stress/measure/stress) technique where the relaxation time was approximately 10 sec between the stress and the measurement stage. Hence, significant relaxation occurred during the early switching cycles which results in recovery of some of the broken interface bonds and hence recovery of interface charge. Figure 4 shows the same gate oxide measured in a package level testing system which has a relaxation between the stress and the measurement cycle of 700 ms. It can be clearly shown that relaxation gives false readings in the early phases of the stress experiment, whereas the degradation curves converge at higher stress levels suggesting that recovery is limited at longer stress intervals.

![Figure 4: NBTI Idsat Degradation for Different S-M-S Methods. Package level (Symbols) and Bench (Lines) Testing Show the Impact of Relaxation at the Early Stress Phases.](image)

The recovery phenomenon has been reported extensively in the literature and was attributed to the re-passivation of the broken Si-H bonds at the Si-Gate oxide interface by molecular hydrogen [14]. Till date it is not exactly clearly understood what the detailed mechanisms are, however, the impact of relaxation can be easily validated by stressing a PMOS transistor and afterwards releasing the stress and measuring the recovery (see Figure 5). Almost 40% of the damage recovers after 30 min of relaxation. Whether to achieve higher level of recovery depends on the local stress equilibrium at the gate oxide and the availability of hydrogen to passivate the Si-H bonds. A simple reaction-diffusion model is commonly used to describe the degradation behavior during NBTI stress [14]. Once the hydrogen has diffused towards the poly gate and sucked away by the polysilicon electrode the hydrogen is lost for future passivation at the gate oxide interface. So it will depend on the level of degradation whether full recovery can be achieved.

To eliminate the relaxation factor from transistor level measurements completed so called “on-the-fly” measurement methods have been established [15][16].
Most “on-the-fly” methods are based on measuring the linear current in a continuous stress condition. It allows to characterize the real degradation behavior of the transistors and represents the circuit situation of a PMOS transistor being stressed over 10yrs lifetime continuously inside the circuit. There are not too many circuits where this situation applies. The majority of the circuits are part of logic or memory cells or regulator circuits. Especially regulators and analog circuits are impacted by NBTI degradation and need to be investigated further. One further interesting observation we would like to present here is the fact that the local equilibrium during the stress phase can adopt very quickly to any change to the equilibrium conditions, i.e. if the stress voltage is lowered during the stress phase spontaneous recovery occurs. Figure 6 gives a PMOS transistor which has been stressed up to a certain stress time at a constant bias and afterwards different stress bias conditions have been applied. It is worth noting that the new equilibrium established fairly quickly and in the case of a lower stress voltage and recovery of NBTI degradation occurred for the 1.35V stress condition. To the contrary, the increased stress voltage of 2.0V caused additional degradation. This finding can be used to design adaptive supply voltages for the PMOS transistors in the individual circuits to increase the circuit level lifetime. One might imagine to lower the supply voltage to certain stress circuits during a standby condition.

The final NBTI degradation on a transistor level depends not only on the gate stress. There are several other components which influence the lifetime such as drain bias, temperature, body bias, duty cycle as well as frequency. All those components can be investigated individually to assemble an analytical NBTI model for circuit design applications. The complete threshold voltage shift caused by NBTI degradation can be calculated to

$$\Delta V_t = K(V_{gs}) \cdot t^k \cdot F(T) \cdot F(V_{ds}) \cdot F(V_{bs}) \cdot F(dcy) \cdot F(W, L),$$  \hspace{1cm} (1)
where K represents the gate voltage prefactor and K0 the power-factor. The gate oxide thickness dependence is not analyzed in this work but also influences the NBTI lifetime significantly. We focus only on the high-performance transistor gate oxide in this work. However, since dual gate oxide technologies are usually manufacturing the thin high-performance gate oxide together with the thick oxide special precaution has to be taken from the standpoint of nitridation. The amount of nitrogen, which blocks boron penetration in the thin gate oxide, might not be optimal for the thick gate oxide. Details of the individual dependencies of the above model have been presented elsewhere [17].

![Figure 6. NBTI degradation dependence on local stress equilibrium. Recovery can be found for switching to lower stress voltages](image)

The local hole concentration can also determine the final NBTI lifetime. For low drain bias conditions (<0.3 Vcc) the depletion region pushes out the holes under the drain edge, hence lifetime improves slightly. If the drain bias is further increased, we enter the hot carrier regime, where the HCI lifetime is significantly impacted by the NBTI phenomena. Usually, HCI testing is not performed at temperature because the lifetime increases due to the degraded mobility and it does not represent the worst case for HCI testing. However, it is not clearly possible to separate the HCI related threshold voltage shift from the NBTI contribution. Figure 7 shows the HCI accelerated lifetime data for different drain as well as gate bias condition. The 10%I\textsubscript{d sat} T50 distribution lifetime is shown with respect to different bias conditions. The conditions for V\textsubscript{ds}=0 represent the pure NBTI stress case, where at V\textsubscript{ds}=Vcc and above a mixed testing regime exists. Sometimes those two components are hard to separate and HCI degradation might convolute the NBTI degradation results.

Another major lifetime factor on the transistor level is the frequency behavior. Since most common products are operated in the multi 100MHz range it is of vital importance to understand the frequency behavior of the individual PMOS transistors. As discussed before, if pauses are applied during the stress cycles the damage can recover and some of the charges dissolve. It is of vital importance to limit the stress pauses always to the same time span in order to draw conclusions between different samples and lifetime tests.
To understand the impact of the duty cycle on the absolute threshold voltage shift we conducted 30%, 70% and 90% duty cycle measurements at 200kHz. The improvement of lifetime with respect to increasing relaxation periods and hence reduction in the absolute threshold voltage shift is depicted in the Figure 8. The lifetime improvement seems to saturate below 30% duty cycling. However, the frequency dependence of this improvement is still under investigation. At higher duty cycles the relaxation periods are not long enough any more and, hence, the lifetime decreases for higher frequency testing.
To further investigate the frequency behavior we are analyzing the individual transistor under DC and AC stress conditions. A typical degradation plots is given in Figure 9, where significant improvement is found for AC stressing. Recently, it has been shown that NBTI lifetime under low frequency stress can be enhanced by a factor of 10 as compared to the DC NBTI lifetime [18,19]. Also depicted are simulation results using a reaction based diffusion model to predict the DC and AC degradation [20]. Good agreement is achieved between experimental and simulation data confirming that the reaction diffusion model is suitable to simulate the NBTI degradation phenomenon.

![Figure 9: NBTI degradation for a DC vs. 200kHz AC signal. Significant improvement is found for AC stressing.](image)

As previously discussed most of the circuits are operating at frequencies above 200kHz so higher frequency data need to be obtained to estimate the frequency dependency. Figure 10 give the single PMOS transistor degradation all the way to 70MHz AC stress frequency. The enhancement in lifetime observed under dynamic stress is in agreement with earlier results [18,19]. A factor of 20X for 1MHz and 100X for 70MHz enhancement in lifetime is observed as compared to the DC stress. This enhancement is attributed to the re-passivation of interface states during the off state and has been explained on the basis of time dependence of the reaction time constant ($k_f$) in the Reaction-Diffusion model [14].

![Figure 10: NBTI degradation for different AC signals. Significant improvement is found for higher AC frequency.](image)
III. Ring Oscillator Reliability

In order to study the effect of higher frequencies on NBTI, ROs with 2 different stage counts were used. In [21], a RO was stressed in DC mode and it was shown that the frequency degradation is directly correlated to the static NBTI stress-induced damage. As mentioned earlier both NBTI and HCI degradation modes may occur in a circuit operation. In a RO HCI degradation occurs during the switching while NBTI takes place when input voltage of the stage, VIN=0. The measured frequency degradation slope for the 100MHz RO is in good agreement with the measured DC NBTI slope, indicating that the RO degradation is dominated by the degradation of PMOS transistors due to NBTI. The Idsat degradation for NMOS device stressed under maximum HCI condition (Vgs=Vdd=2.0 V) (see Figure 11). The degradation was monitored during stress to eliminate any possible relaxation. The obtained HCI degradation slope is 0.4, consistent with earlier results. Since the HCl damage occurs only during switching events, the obtained DC Idsat HCI should be scaled to obtain the HCI contribution to RO degradation. The contribution of HCI is a strong function on frequency as at higher frequency more switching events occur. For PMOS devices, DC NBTI was measured at two different temperatures with Vgs=-2 Vand Vds=-0.1 V as shown in Figure 11. The obtained degradation slope at 25°C and 175°C is 0.1 to 0.12. Since the temperature dependence of HCI is very weak, it can be seen that at 25°C even after scaling for degradation during switching event, there will be a small contribution from HCI. Notice at 175°C, the HCI degradation measured on PMOS devices is larger than HCI degradation measured on NMOS devices. Therefore, the NBTI component will dominate the RO degradation at 175°C as will be shown further.

![Figure 11: Idsat degradation for PMOS devices during NBTI stress at 25°C and 175°C (Vgs=-2 V and Vds=-0.1 V) and Idsat NMOS HCI degradation at 175°C. For HCI stress condition was Vg=Vd=2 V.](image)

In Fig. 12, the frequency degradation at 175°C is shown for both the 100MHz and 3GHz ROs. Three observations can be made from this data: (1) A 4 decade improvement in lifetime is observed for ROs as compared to DC-stressed devices. (2) From 100 MHz to 3 GHz, the frequency-dependence of NBTI degradation is a weak function of the RO frequency. (3) As compared to DC data at 175°C, a higher degradation slope is measured for both 100 MHz and 3 GHz RO frequency degradation.
This latter observation cannot be attributed to HCI since the 100 MHz RO should exhibit 30x less damage compared to the 3 GHz RO. Therefore, similar to the RO degradation at 25°C we should obtain a small difference in slopes and amount of degradation. At higher temperature hydrogen diffusion is faster. One possible explanation for higher slope at high temperatures is the loss of hydrogen via a lock-in mechanism. In this case, the generated hydrogen has diffused out of the oxide and is no longer available for re-passivation [22]. Since the DC degradation slope shows weak temperature dependence, the loss of hydrogen into poly via a lock-in type mechanism can not explain the higher slope of the RO data. It is proposed that the relaxation at 175°C is enhanced when the VIN=1.2V. This would increase the degradation slope as discussed earlier for the stress-sense technique. The weak frequency dependence between 100MHz and 3GHz indicates that a critical timescale of the degradation mechanism is reached. The lower degradation for RO frequency implies a larger reliability margin for continuously switching circuits than individual transistors would predict.

![Graph showing RO frequency degradation at 175°C. Also shown is the Idsat degradation for DC stress on a PMOS transistor at the same temperature.](image)

**IV. Product Level Reliability**

Since today’s products operate at elevated temperatures and complicated stress schemes (AC vs. DC) and different power domains product level reliability at operating temperature is becoming increasingly important. Typical HTOL “Hot Temperature Operating Life” tests are common in the industry. During HTOL testing the product is brought up to elevated temperature and the devices are toggled or tested with a certain product speed at accelerated supplies. Previously, only gate oxide reliability as well as hot carrier reliability was of concern. Now NBTI adds a significant reliability concern to the overall lifetest. It is important to be able to simulate the impact of NBTI on a circuit level using SPICE simulators. The above described NBTI model (Eq.1) can be implemented as procedural function call during the netlist extraction sequence. The procedural interface needs also the cycling information from circuit simulations (Verilog level). Each transistor model can be changed individually by adjusting the threshold voltage in the SPICE model. Alternatively, all transistor corners might be shifted together as a worst case estimate. Compared to HCI reliability it is difficult to identify
NBTI critical circuitry. However, DC biased circuits such as regulators and analog circuitry are more prone to NBTI degradation and need to be identified as early as possible in the design cycle.

In order to prove product level reliability with respect to HCI “Low Temperature Operating Life” test capture pretty well the HCI degradation and operate the circuits at reduced switching speed to modulate HCI. For NBTI degradation, however, it is very difficult to find the right operating condition since voltage, temperature and relaxation dependence play a huge role. Typically one might assume a DC stress (IO’s grounded or high) at elevated temperature and supply voltage might mimic the worst case circuit condition stress, however, if the product has a regulator the output voltage of such regulator usually droops because of the current it has to supply. Hence the individual transistors are stressed at lower voltages, which does not represent the worst case condition. On the other hand during standby the output voltage of the regulator might be at maximum bias, however, the temperature can be significant below max operating temperature. Generally it is very difficult to find appropriate product parameters to characterize NBTI degradation and not to incur any relaxation. However, so is the real product under nominal operation and some of the product level test are still valid tests because they reflect the real operating conditions in the field.

Figure 13 shows the product level NBTI stress data for a low power asynchronous SRAM memory. We selected the access time as quality criterion to evaluate the NBTI lifetime. The memory is stressed at constant accelerated DC bias and temperature and different readpoints are acquired for the access time $T_{aa}$ at 0.5, 1, 2, 3 and 4 hours. The $T_{aa}$ pushout caused by NBTI stress is then used to extract the lifetime using a power law dependence.

![Figure 13: ASYN SRAM MEMORY $T_{aa}$ PUSHTOUT DUE TO NBTI STRESS FOR DIFFERENT TEMPERATURES AND STRESS VOLTAGES.](image)

Figure 13 reflects well the NBTI related degradation behavior. The lifetime slope was correlated to single transistor data and showed good agreement. The most difficult part of product level testing is to identify a product parameter which reflects NBTI stress degradation and does not show excessive recovery which might not represent worst case operating conditions.
Conclusions

We presented a comprehensive analysis of the major reliability concerns for deep submicron technologies. HCI reliability has become less of a concern for state-of-the-art technologies, where NBTI has risen to the major reliability challenge. We presented a detailed analysis of the relaxation and degradation behavior of NBTI on transistor, small circuit as well as product level. Depending on the bias conditions, temperature, and duty cycling a certain absolute threshold voltage shift can vary widely. RO data as well as product level data suggest a wider margin might exist for the whole integrated circuit compared to the individual transistor based on the fact that relaxation significantly allows for charge recovery. In the real circuit application there is hardly any real DC condition over the whole life of the product. Further studies are necessary to complete understand the linkage of transistor level degradation to product level degradation.

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References