Integrated Low-Loss CMOS Active Rectifier for Wirelessly Powered Devices

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Abstract—A low-loss CMOS full-wave active rectifier is presented. It consists of two dynamically biased and symmetrically matched active diodes each realized by an NMOS switch driven by a 2ns voltage comparator with reverse current control. With a load of 1.8kΩ, the rectified DC voltage is 3.22V and 1.2V for a 13.56MHz AC sinusoidal input voltage of 3.5V and 1.5V respectively. It is fabricated in a 0.35μm CMOS process with an active area of 0.0055mm², with no low-threshold devices and on-chip passive components.

Index Terms—AC-DC power conversion, radio-frequency identification (RFID), rectifiers, symmetrical matching, wireless power transmission

I. INTRODUCTION

Wireless devices such as biomedical implants [1]-[4] and RFID tags [5, 6] are powered by a wireless inductive link. Without an embedded battery, they can only be activated when placed near the transmitter. Fig. 1 shows the block diagram of a generic wirelessly powered system. The inductive coil or antenna captures the RF signal. The coupled energy is then passed to a resonance tuning circuit to generate a high AC voltage, followed by a rectifier to convert it into a DC voltage to power up the signal processor downstream. A rectifier with high efficiency is then essential in extending the reading distance and reducing the power requirement of the transmitter.

AC to DC conversion is conveniently achieved by diodes and capacitors. Single-diode half-wave rectifier is simple and full-wave rectifier with a diode bridge (Fig. 2(a)) makes better use of the AC input and gives a smaller output ripple voltage. They are commonly used in high voltage applications where the diode forward voltage drop of 0.7V to 1V is relatively low. However, for low voltage integrated circuit applications, this forward drop significantly reduces the power conversion efficiency (PCE). Schottky diodes with a low forward drop could be used to enhance the efficiency. However, the production cost is high compared to a standard CMOS process. In a CMOS-only implementation, the diodes can be replaced by diode-connected MOS transistors. Low threshold voltage (Vt) transistors could be used in advanced CMOS processes, requiring extra cost for additional masks and fabrication steps. Alternatively, Vt cancellation technique in standard CMOS processes [7, 8] could reduce the turn-on threshold by additional biasing circuits. In both cases, the gate-to-drain voltages are fixed and the gate-drive voltages are controlled by their drain-to-source voltages that change only slightly from forward to reverse conduction. Therefore, the switches cannot be turned on and off completely and this leads to inefficient rectification.

In [9], two diodes of the diode bridge rectifier are replaced by two cross-coupled PMOS transistors (Fig. 2(b)). The gates of these PMOS transistors are driven by a larger voltage swing than diode-connected PMOS transistors and hence a higher on/off current ratio can be achieved. However, the bottom two diodes are still implemented by diode-connected NMOS transistors to block the reverse current, and the efficiency is not optimized. It would be advantageous if the diodes could be replaced by active circuitries that can be turned on fast when $|V_{AC}| > V_{DC}$, and turned off fast to avoid reverse current leakage.

On-chip active rectification has been demonstrated in a highly efficient voltage doubler [10] by using active diode circuitries instead of passive diodes. High power conversion efficiency was achieved when operating at 1MHz. However, many wirelessly powered devices operate at a much higher frequency, for example, in the 13.56MHz ISM (Industrial, Scientific and Medical) band. Moreover, the generation of the biasing current is not trivial, as there is no DC supply when the wireless device is initially relaxed.

In this research, a low-loss CMOS active rectifier is presented. All the four power transistors are driven on and off completely.
II. SWITCHING DYNAMICS OF ACTIVE RECTIFIER

To enhance the efficiency, we propose a full-wave active rectifier employing active diodes with very low forward drop to replace the bottom diodes of [9], as shown in Fig. 3(a). Now, D1 (equivalently, MN1) should be turned on when \( V_{C2} - V_{C1} > V_{DC} - V_{GND} \), or

\[
V_{C2} - V_{DC} > V_{C1} - V_{GND} \tag{1}
\]

The switching dynamics is discussed below. Fig. 4 shows the simulated waveforms of VC1 and VC2 together with VDC, |VAC|, and VGND (the 0V line) for study. From Fig. 4, we observe that the waveforms V C1 and V C2 together with V DC (solid black line), |V AC| (solid grey line) and VGND (the 0V line) look more like skewed and distorted sinusoids. The switching dynamics is discussed below.

When \( V_{C1} > V_{C2} \), D1 is reverse-biased and is off, cutting the return path for MP4, and so MP4 is also off. This half period, four transitions resulting in 5 states can be identified. At the start of the period \( t = T_{00} \), V AC = 0, and all PMOS and diodes are off. When \( V_{C1} - V_{C2} = |V_{tp}| \) at \( t = T_{01} \), MP4 is gradually turned on, shorting V C1 to V DC. As such, the change in V AC is reflected by the drop in V C2. It should be noted that as D2 is not turned on, no drain current flows in MP4. At \( t = T_{02} \), V AC is higher than V DC such that V C2 drops below V GND, and the diode D2 (with a very low forward drop) is then turned on. V DC is charged up via D2 and MP4, and conduction drop can be observed due to their finite resistance (Fig. 4). After V AC reaches the peak, it starts to decrease and at \( t = T_{03} \), V C2 rises above V GND, turning off D2. As V AC drops to \( |V_{tp}| \) at \( t = T_{04} \), the gate drive of MP4 is insufficient to short V C1 to V DC, and V C1 starts to drop. All PMOS and diodes are off for the rest of the half period. The operation of the rectifier in the second half period is similar to that of the first half period, except that MP3 and D1 are responsible for the action. Table I tabulates all the switching actions in one complete period.

<table>
<thead>
<tr>
<th>State</th>
<th>D1</th>
<th>D2</th>
<th>MP3</th>
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<td>S00</td>
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<td>S14</td>
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With a V AC of 3V and a load resistor of 1.8kΩ, the ideal full-wave rectifier gives a V DC of 2.75V. However V DC drops to 2.23V if the idealized diodes are replaced with diode-connected NMOS transistors, as shown in Fig. 5, giving a lower efficiency.
Therefore, it is natural to employ common-gate structures for the input stages of the comparator to satisfy the above requirements. Transistors M1 to M4 serve as a 2-stage comparator with common-gate input stages. The low-side common-gate input stage formed by M1, M2 and M3 monitors the voltage across MN1. The high-side input stage formed by M3, M4 and M5 monitors the voltage across MN2. The source of M4 is connected to VC2 instead of VDC to serve two purposes. First, when the rectifier is relaxed, VDC = 0V. The rectifier cannot start up when the source of M4 is connected to VDC. For the present connection, D1 will be activated whenever VC2 > |Vtp| + Vtn. Second, the bias current of the comparator will be zero when VC2 swings below |Vtp| + Vtn (due to the diode-connected M4 and M2) or 2|Vtp| (due to M4 and M5). As a result, only one active diode is activated at a time and the quiescent current is reduced. Hence, dynamic biasing is realized and with no extra startup circuitry. M5 works as a bias limit resistor.

When two NMOS (or PMOS) transistors are matched, they have the same W/L ratio. When they are symmetrically matched, in addition to having the same W/L ratio, their respective drain, gate and source voltages are forced to be the same by proper biasing. Now, transistors M1, M3 and M5 are symmetrically-matched with M2, M4 and M6 to achieve low systematic offset. Transistor M6 also serves two purposes. First, it is used to match the bias-limiting transistor M6. Second, it serves as a resistor such that VAP and VAN rise faster to turn off MN1 earlier before it would be reversely biased, thus achieving reverse current control (RCC). This technique effectively compensates for the delay of the comparator. Measurement results in Sec. IV show that under the same input AC voltage magnitude and loading condition, the rectifier with RCC produces a larger DC output voltage, higher power conversion efficiency and a lower output ripple voltage.

IV. SIMULATION AND MEASUREMENT RESULTS

The proposed full-wave active rectifier was fabricated in a 0.35μm 4-Metal/2-Poly CMOS process, and the micrograph is shown in Fig. 7. The active area is 0.0055mm² (0.1065mm² including pads). All transistors (except M5, M6 and M9 in D1 and D2) have minimum channel length to maximize the operation speed. The chip was carefully layout to have a symmetrical structure in minimizing potential unbalance in parasitic capacitances between VC1 and VC2. An active rectifier without RCC (i.e., without M6) was also fabricated for comparison.

To mimic the operation environment for measuring the performance of the active rectifier, an inductive power link was used as the AC source. The inductive coupling links of the active rectifier are shown in Fig. 8. The proposed full-wave active rectifier was tested on the inductive power link with 4 sinusoidal voltages VC1 and VC2 to ensure that the rectifier could start up before VDC is charged up.
set up, as shown in Fig. 7. Two rectangular coils (50mm x 60mm), each with 3 turns, were etched on two PCBs. The measured inductance of each coil was around 900nH. A signal generator was used to drive the primary coil on PCB 1 with a 13.56MHz sinusoidal signal, and energy was then transferred to the secondary coil by inductive coupling. The two coils were aligned and separated by 50mm to reduce capacitive coupling. A filtering capacitor $C_O$ of 200pF and a load resistor $R_L$ of 1.8kΩ were mounted on the secondary side (PCB 2). The coil with added resonance capacitors and parasitic capacitors of probes were designed to resonate at around 13.56MHz. An SOIC package was used for the fabricated active rectifier and the chip was mounted on PCB 2. Measurements were taken by three probes with ground terminals connected to $V_{GND}$ of the active rectifier. The voltage across the secondary coil at resonance ($V_{AC}$) was obtained by subtracting $V_{C2}$ from $V_{C1}$.

Fig. 8 shows the measurement results of the proposed active rectifier without RCC. Fig. 8(a) shows that the waveforms of $V_{C1}$ and $V_{C2}$ are similar with a phase shift of 180°, meaning that the active diodes $D_1$ and $D_2$ are well matched in on/off thresholds and turn-on/off times. The zoom-in waveform in Fig. 8(b) shows the details of the first half cycle ($V_{C1} > V_{C2}$). A delay of less than 2ns is observed for turning on $MN_2$ of $D_2$. When $MN_2$ is on, a large current passes through $MP_4$ and $V_{C1}$ is then higher than $V_{DC}$, starving the current of $M_3$ in $D_2$, and makes $V_{AP}$ and $V_{AN}$ to drop fast, and turns on $MN_2$ fast. Note that $V_{C1}$ drops below $V_{DC}$ before $MP_4$ is turned off, lowering the rectified DC voltage and thus the efficiency.

Fig. 9 shows the measurement results of the active rectifier with RCC. It has a similar turn-on characteristic with the previous case. The addition of $M_9$ helps to deliver more current to $M_3$ (through $M_4$), thus charging up $V_{AP}$ and $V_{AN}$ earlier, and turns off $MN_2$ fast to prevent reverse current. This action is demonstrated by observing $V_{C1}$ and $V_{DC}$ in Fig. 9(b). $V_{C1}$ does not drops below $V_{DC}$ when $V_{DC} - V_{C2}$ (gate drive voltage of $MP_4$) is larger than $|V_{tp}|$. By comparing the $V_{DC}$ waveforms in Fig. 8(b) and Fig.9(b).
and Fig. 9(b), we conclude that the RCC scheme reduces the ripple voltage by half, and a higher DC voltage is obtained. Note that the peak of \( V_{AC} \) waveform shown in Fig. 9(a) is flattened due to the current drawn from the secondary coil with finite resistance.

Fig. 10 shows the measurement result of the conversion ratio \( M = \frac{V_{DC}}{|V_{AC}|} \) versus the magnitude of the AC input. With the RCC, when the AC input is 3.5V, \( V_{DC} \) is 3.45V when unloaded (\( M = 0.986 \)) and 3.22V with \( R_L = 1.8k\Omega \) (\( M = 0.929 \)). Without RCC, \( V_{DC} \) drops to 3.25V when unloaded (\( M = 0.886 \)) and 3.1V with a \( R_L = 1.8k\Omega \) (\( M = 0.868 \)). The RCC scheme is effective in reducing the dropout voltage, even when the AC input is lower than 2V. The rectifier works well with an AC input voltage as low as 1.5V and a frequency up to 20MHz. The ideal case shown in Fig. 3(b) with cross-coupled PMOS transistors, ideal diodes, and \( R_{ON} = 0.1\Omega \) were also simulated with no load and a load of 1.8k\( \Omega \). The performance of the proposed rectifier with RCC is closer to the ideal case, especially at a high input AC voltage magnitude, because a larger bias current and a larger gate-drive voltage are achieved. Table II summarizes the design parameters and the performance of the proposed active rectifier.

Power conversion efficiency PCE of the proposed rectifier is simulated and the results are shown in Fig. 11. With \( R_L = 1.8k\Omega \), the PCE is larger than 87% for an AC input of higher than 2V. Without RCC, PCE is worse, especially at a low AC input voltage, due to a larger reverse current leakage.

Fig. 12 shows the measured conversion ratio \( M = \frac{V_{DC}}{|V_{AC}|} \) versus input frequency at \( |V_{AC}| = 3.5V \) and \( R_L = 1.8k\Omega \). In the original design, \( C_O = 200pF \) is optimized for 13.56MHz operation. For lower operating frequency, larger \( C_O \) (2nF) is required to maintain high conversion ratio.

V. CONCLUSIONS

An integrated CMOS active rectifier for wirelessly powered devices is presented. A 4-input comparator with common gate input stages is proposed to effectively drive an NMOS power switch with a performance that matches a zero-threshold diode. Measurement results show that the proposed rectifier has a turn-on delay of less than 2ns and reverse current is effectively eliminated by a simple reverse current control scheme. The proposed design could be employed in wirelessly powered biomedical implants and passive RFID tags.

Fig. 10. Measured voltage conversion ratio \( M = \frac{V_{DC}}{|V_{AC}|} \) versus \(|V_{AC}|\) at \( f_I = 13.56MHz\): (a) with RCC & unloaded, (b) with RCC & \( R_L = 1.8k\Omega \), (c) without RCC & unloaded, (d) without RCC & \( R_L = 1.8k\Omega \). Grey lines are simulation results of the rectifier (e) with ideal diodes & unloaded and (f) with ideal diodes & \( R_L = 1.8k\Omega \).

Fig. 11 Simulated power conversion efficiency versus \(|V_{AC}|\), \( R_L = 1.8k\Omega \).

Fig. 12. Measured conversion ratio of the proposed rectifier with the change of input frequency.

![Figure 11](image1.png)

![Figure 12](image2.png)

REFERENCES


