Fast Simulation of Hybrid CMOS and STT-MTJ Circuits with Identified Internal State Variables

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Abstract—Hybrid integration of CMOS and non-volatile memory (NVM) devices has become the technology foundation for emerging non-volatile memory based computing. The primary challenge to validate a hybrid system with both CMOS and non-volatile devices is to develop a SPICE-like simulator that can simulate the dynamic behavior of hybrid system accurately and efficiently. Since spin-transfer-torque magnetic-tunneling-junction (STT-MTJ) device is one of the most promising candidates of next generation NVM devices, it is under great interest in including this new device in the standard CMOS design flow. The previous approaches require complex equivalent circuits to represent the STT-MTJ device, and ignore dynamic effect without consideration of internal states. This paper proposes a new modified nodal analysis for STT-MTJ device with identified internal state variables. As demonstrated by a number of experiment examples on hybrid systems with both CMOS and STT-MTJ devices, our newly developed SPICE-like simulator can deal with the dynamic behavior of STT-MTJ device under arbitrary driving condition and reduce the CPU time by more than 20 times for memory circuits when compared to the previous equivalent circuit approaches.

I. INTRODUCTION

The recent advance in nonvolatile memory (NVM) has introduced promising future for new computing systems as the nonvolatile property can lead to fast access time, low energy and high integration density. A range of NVM devices [1-3] such as Memristor, Phase Change Random Access Memory (PCRAM) and Magneto-resistive Random Access Memory (MRAM), have been developed to potentially replace both Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) in the conventional computing system. Especially, spin-transfer-torque magnetic-tunneling-junction (STT-MTJ) device based MRAM has reduced cell size 3-4 times to about 6-8F² (F is the minimum technology dimension,~0.4µm) [4] compared to the traditional MRAM devices. Such advantage can be further enhanced with 3DIC stacking [5].

In the emerging NVM technologies, very often new devices cannot be fully described by the conventional circuit state variables such as nodal voltage or branch current. For instance, an additional internal state variable called magnetization has to be added to describe the dynamic behavior of STT-MTJ. The previous approaches describe STT-MTJ by equivalent circuit [6-8] with additional circuit components and hence increased complexity. One limitation of equivalent circuit approach is many additional circuit components are required to maintain high accuracy when dealing with the dynamic behavior of internal state variables. As such, the computation efficiency of equivalent circuit is not high and lack of scalability. One equivalent circuit may require dozens of extra circuit components to describe one STT-MTJ device, and hence results in huge overhead to model and simulate large-scale memory designs. As such, novel modeling and simulation techniques are needed to improve the computation efficiency for the memory circuits with CMOS and STT-MTJ devices.

In order to consider new non-volatile devices similarly to how we dealt with CMOS devices by physics based model, one critical perspective is to identify and include the new state variable relevant for the new dynamic behavior of the non-volatile devices. Note that different from device parameter, a device state variable varies with time under given input signals. Here, we deploy the term "internal state variables" to represent those physics based variables, while the conventional state variables such as nodal voltage and branch current are named "external state variable". Take STT-MTJ for instance, many variables can be extracted from the physics point of view, such as temperature, polarization, magnetization, etc. Variables like temperature and electron polarization are assumed to be constant or parameters. But the variable of magnetization is the state associated with STT-MTJ and can change with time similar to the states of nodal voltages and branch currents. As such, the angles to describe magnetization are identified as internal state variables for STT-MTJ devices.

In this paper, we have the following primary contributions: (1) internal state variables have been identified for the consideration of nonlinear dynamic models of STT-MTJ devices; and (2) a new modified nodal analysis (MNA) formulation has been developed to consider internal state variables of STT-MTJ devices within one SPICE-like simulator. Experiments show that our new MNA formulation with internal state variable can handle the simulation of timing, power, variation and detailed transient behavior for the hybrid design of STT-MTJ devices with CMOS at large scale. Compared to equivalent circuit approaches that only work for constant current driving condition, the newly developed SPICE-like simulator can be used to study the device dynamic behavior under arbitrary driving condition, and the CPU time can be reduced by more than 20 times.

The rest of this paper is organized in the following manner. In Section II, the STT-MTJ device model with internal state variables is discussed. In Section III, the general derivation of a new MNA formulation to consider internal state variables of STT-MTJ is then introduced. Experimental results are presented in Section IV with conclusion in Section V.
II. DEVICE MODELING WITH INTERNAL STATE VARIABLES

In this section, the operation of STT-MTJ device is discussed. Then the internal state variables of STT-MTJ devices are identified as magnetization angles with the consideration of arbitrary driving condition. All variables used in this section are summarized in TABLE I.

### TABLE I

<table>
<thead>
<tr>
<th>Variables</th>
<th>Definitions</th>
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<tbody>
<tr>
<td>$\theta$ and $\phi$</td>
<td>shown in Figure 2, azimuthal angles of magnetization orientation in x-y and y-z plane.</td>
</tr>
<tr>
<td>$R_{H}, R_{L}$</td>
<td>resistance values of anti-parallel state and parallel state</td>
</tr>
<tr>
<td>$\Delta R_{GMR}$</td>
<td>difference between $R_{H}$ and $R_{L}$</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>damping constant</td>
</tr>
<tr>
<td>$e$</td>
<td>charge of electron</td>
</tr>
<tr>
<td>$A$</td>
<td>area of STT-MTJ cross-section</td>
</tr>
<tr>
<td>$I_{m}$</td>
<td>thickness of oxide barrier</td>
</tr>
<tr>
<td>$H_{A}, H_{K}$</td>
<td>applied field and effective anisotropy field</td>
</tr>
<tr>
<td>$M_s$</td>
<td>saturation magnetization of material</td>
</tr>
<tr>
<td>$\tau$</td>
<td>normalized time, $\tau = \gamma_e \cdot M_s \cdot t$</td>
</tr>
<tr>
<td>$\Delta$</td>
<td>thermal stability factor</td>
</tr>
<tr>
<td>$\tau_0$</td>
<td>inverse of attempt frequency (~1ns)</td>
</tr>
<tr>
<td>$I_c$</td>
<td>critical current of spin transfer transfer</td>
</tr>
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</table>

Figure 1. (a) Typical STT-MTJ structure and state change diagram; and (b) V-R curve of STT-MTJ device.

A typical STT-MTJ device structure appears as a sandwich with two ferromagnetic layers and one oxide barrier in between [9-11]. One STT-MTJ device has two stable states: parallel state (P) or anti-parallel state (AP), where the free layer magnetization is in the same or the opposite direction with hard axis (magnetization direction of fixed layer), respectively. One giant magneto resistance (GMR) at AP state ($R_H$) is higher than the GMR at P state ($R_L$)[12]. The angle $\theta$ is one magnetization angle between free layer and hard axis, and the GMR can be expressed as [13]:

$$R(\theta) = R_L + \frac{R_H - R_L}{2} (1 - \cos \theta)$$

$$= R_L + \frac{\Delta R_{GMR}}{2} (1 - \cos \theta)$$  \hspace{1cm} (1)

It can be easily derived from (1) that: $R_{\theta=0} = R_L$ at P state and $R_{\theta=\pi} = R_H$ at AP state.

The operating principle of STT-MTJ device can be summarized as: the external current induces the state (P or AP) change. As depicted in Figure 1(a), STT-MTJ is switched from P to AP with sufficient forward biased current and from AP to P with sufficient reverse biased current. In order to model this mechanism accurately, we need to look into two dominant effects in the device physics of STT-MTJ: tunneling effect [11], and spin transfer torque effect [10].

Tunneling effect of STT-MTJ can be understood as a parabolic relationship between the junction conductance and the applied voltage [11]. This relationship is illustrated by line segments 'ab' and 'cd' in Figure 1(b), which represent the change of normalized resistances with voltage at P and AP states, respectively. Tunneling effect becomes dominant when the applied voltage is relatively small such that it will not trigger the STT-MTJ to change state. This relation can be approximated by:

$$R_L (V) = \frac{R_L(V=0)}{1 + k_a V^2}; \quad R_H (V) = \frac{R_H(V=0)}{1 + k_b V^2},$$  \hspace{1cm} (2)

where $k_a$ and $k_b$ are voltage-dependent coefficients for parallel state and anti-parallel states, respectively.

Spin transfer torque effect becomes dominant when the current flowing through the STT-MTJ is larger than the critical value ($I_c$). This relationship is illustrated in the line segments 'bc' and 'da' in Figure 1(b). When the current at the junction is higher than the critical value ($I_c$), the resistance will switch between $R_H$ and $R_L$ regions. This process is called magnetization reversal. However, magnetization reversal is not an instantaneous process. The switching time required ($T_s$) for magnetization reversal decreases exponentially with the current applied ($I_0$) [7]:

$$T_s = \tau_0 e^{\Delta (1 - \frac{I_0}{I_c})}$$  \hspace{1cm} (3)

where $I_c$ is the switching time at $I_0 = I_c$, and the definitions of remaining variables are in TABLE I. Note that $T_s$ from (3) is the minimum pulse width requirement for certain $I_0$. For particular write-operation in STT-MTJ device based memory, one must make sure that the constant current larger than $I_c$ is applied within a period of $T_s$.

The better understanding $T_s$ is important for modeling STT-MTJ devices. This requires the analysis for the dynamic behavior of STT-MTJ device under arbitrary driving condition. The Landau-Lifshitz-Gilbert equation (LLG) [10] is deployed for this purpose:

$$\frac{dm}{d\tau} = -m \times [h + \chi(m \times p)] + a \left( m \times \frac{dm}{d\tau} \right),$$  \hspace{1cm} (4)

where $\chi$ is pre-factor of the spin transfer term, $p$ is the hard axis unit vector, and the definitions of remaining variables are shown in TABLE I.

The solution of (4) can be interpreted as the change of the normalized magnetization ($M$) of free layer over time. $M$ can be expressed in spherical coordinates with variables $\phi$ and $\beta$ as shown in Figure 2. $\theta$ and $\phi$ are the azimuthal angles of $M$ in x-y plane and y-z plane, respectively, and $\beta$ is the elevation angle of $M$ from x-y plane. Note that for a very thin free layer, the value of $\beta$ is rather small and will not affect the modeling of
STT-MTJ. So only \( \theta \) and \( \phi \) are associated with the dynamic state of STT-MTJ device, describe the normalized magnetization direction, and are calculated by [10]:

\[
\theta = \theta_0 \exp \left( -\frac{t}{\tau_0} \right) \cdot \cos(\phi),
\]

\[
\omega = \frac{d\phi}{dt} = k_c \sqrt{k_d} - (\chi_{\text{crit}} - k_d)^2,
\]

where \( \theta_0 \) is the initial value of \( \theta \), which is slightly tilted from P or AP directions; \( \tau_0 \) is precession time constant; and \( \omega \) is the angular speed of \( \phi \); \( k_c = y_0 \cdot M_s \) is product of gyromagnetic ratio and saturation magnetization; \( k_d \approx \frac{y_k}{M_s} \) is a function of anisotropy and applied field; \( \chi_{\text{crit}} \) is the critical pre-factor of spin transfer term, which is around half of the damping constant; \( k_e \) is the ratio between pre-factor of the spin transfer term and driving current. Definitions of remaining variables are shown in TABLE I.

Figure 2. STT-MTJ magnetization of free layer in spherical coordinates with three magnetization angles: \( \theta \), \( \phi \) and \( \beta \).

As such, with the consideration of tunneling effect, spin transfer torque effect and arbitrary driving condition, the dynamics of one STT-MTJ device model can be estimated with equations (1), (2), (5) and (6), linking internal state variables \( \theta \) and \( \phi \) with the external state variables (nodal voltage and branch current). Previous approaches by equivalent circuit [6-8] require the use of quite a number of additional circuit components to capture this dynamics and have high complexity for large-scale simulation and model. For instance, as depicted in Figure 3, to implement an equivalent circuit of STT-MTJ shown in [8], at least 10 more circuit elements have to be added, including current control current source, capacitor, decision circuit and curve fitting circuit, etc. As a result, the circuit overhead of equivalent circuit approach can grow as the circuit size increases, which leads to huge amount of computation time.

III. SIMULATION WITH INTERNAL STATE VARIABLES

In this paper, we show that a new modified nodal analysis (MNA) can be applied to consider internal state variables for STT-MTJ device in SPICE-like simulator. As such, it can provide compact physics-based description for internal states with high efficiency and accuracy. All the relevant variables used in this section are summarized in TABLE II.

<table>
<thead>
<tr>
<th>Variables</th>
<th>Definitions</th>
</tr>
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<tbody>
<tr>
<td>( s_m )</td>
<td>internal state variable for new MNA</td>
</tr>
<tr>
<td>( v_a, f_0 )</td>
<td>traditional state variables for MNA: nodal voltage and branch current</td>
</tr>
<tr>
<td>( v_n, j_n )</td>
<td>branch voltage, source current, and inductor current</td>
</tr>
<tr>
<td>( G, C, L )</td>
<td>traditional conductance, capacitance and inductance</td>
</tr>
<tr>
<td>( S )</td>
<td>new Jacobian as memductance</td>
</tr>
<tr>
<td>( K^c_c, K^f_f, K^g_g, K^i_i )</td>
<td>new Jacobians introduced by ( s_m )</td>
</tr>
<tr>
<td>( E_c, E_g, E_f )</td>
<td>incident matrix for capacitor, resistor, inductor and current source</td>
</tr>
<tr>
<td>( E_{in} )</td>
<td>new incident matrix introduced for NVM devices</td>
</tr>
<tr>
<td>( f, g )</td>
<td>functions introduced by ( s_m ) for new state equations</td>
</tr>
<tr>
<td>( \omega_{\phi} )</td>
<td>angular movement speed of ( \phi )</td>
</tr>
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</table>

A. New MNA with Internal State Variables

In order to handle the dynamic models of NVM device with internal state variables, one can develop a new MNA by adding the internal state variables into the traditional MNA for CMOS devices. As shown in Figure 4(a), these internal state variables, termed as \( s_m \), determine the conductance of non-volatile devices, termed as memductance (memory conductance) here, and therefore can be categorized as one new device branch.

Figure 4. New MNA with: (a) components and state variables; (b) large signal KCL; and (c) small signal KCL.

We should note that the simulation time is directly related to the total number of state variables generated for the circuit. Compared to the traditional approaches with complex equivalent circuits, the introduction of memductance adds much fewer state variables by including internal state variables to describe dynamic effect of NVM device. In the case of STT-MTJ, its equivalent circuit requires dozens of additional nodal voltages to characterize the circuit behavior, while only two nodal voltages and two internal state variables are required in our memductance approach. Therefore, the introduction of memductance greatly simplifies the model complexity and in turn largely reduces the verification and design cost.

Note that one NVM device may require one or multiple internal state variables to accurately describe its dynamic behaviors, e.g. \( \theta_m \) and \( \phi_m \) for STT-MTJ. The according incident matrix is termed as \( E_{in} \), with which the non-volatile device branch current is obtained as \( E_{in} \left( E_{in}^m v_n, s_m, t \right) \). As
Figure 4(b) shows, combined with branch currents from the traditional CMOS devices, a new KCL equation is formed by

\[
\frac{d}{dt}E_q(E_v^T v_n, t) + E_m(E_v^m v_n, s_m, t) + E_g(E_g^T v_n, t) + E_j^i + E_j^i = 0;
\]

\[
L_i \frac{d}{dt}j_i - E_v^i v_n = 0; \quad E_v^i v_n = 0;
\]

\[
f(E_v^m v_n, s_m, t) + \frac{d}{dt}g(E_v^m v_n, s_m, t) = 0.
\]

(7)

Here functions \(f\) and \(g\) are the additional state equations for non-volatile devices with \(s_m\). Moreover, with the new state variable vector \(X = [v_n, j_i, j_i, s_m]^T\), the above new MNA can still be described by the differential-algebra-equation (DAE) as

\[
F(x, \dot{x}, t) = \frac{d}{dt}q(x, t) + j(x, t) = 0
\]

(8)

We can further derive the Jacobian or generalized conductance \(G\), capacitance \(C\), and memductance \(S\). The additional term of memductance \(S\) is introduced to describe the conductance of non-volatile devices for the induced current change under the change of internal states. At one biasing point \(X_0\), the first-order derivative or Jacobian of the new DAE with respect to \(X\) is given by

\[
G = \left( E_g \frac{d}{dv^g} [v_g^T, t] E_g^T + E_m \frac{d}{dv^m} m [v_m^m, s_m, t] E_m^T \right)_{x=X_0};
\]

\[
C = \left( E_c \frac{d}{dv^c} [v_c^T, t] E_c^T \right)_{x=X_0};
\]

\[
S = \left( E_m \frac{d}{ds_m} [v_m^m, s_m, t] E_m^T \right)_{x=X_0},
\]

(9)

where \(v^g = E_g^T v_n, v^m = E_m^T v_n, v^c = E_c^T v_n\).

In addition, there are four additional Jacobian terms introduced from functions \(f\) and \(g\) due to the new state variable \(s_m\) for non-volatile device:

\[
\mathcal{K}_v^F = \left( E_m \frac{d}{dv^m} f(v_m^m, s_m, t) E_m^T \right)_{x=X_0};
\]

\[
\mathcal{K}_v^G = \left( E_m \frac{d}{ds_m} g(v_m^m, s_m, t) E_m^T \right)_{x=X_0};
\]

\[
\mathcal{K}_s^F = \left( E_m \frac{d}{dv^m} f(v_m^m, s_m, t) E_m^T \right)_{x=X_0};
\]

\[
\mathcal{K}_s^G = \left( E_m \frac{d}{ds_m} g(v_m^m, s_m, t) E_m^T \right)_{x=X_0}.
\]

(10)

The subscripts \(v\) and \(s\) denote the derivatives to non-volatile device branch voltage \(v_m^m\) and its internal state variable \(s_m\), respectively. The superscript \(F\) and \(G\) correspond to functions \(f\) and \(g\), which are current and charge terms for the KCL equation, respectively.

With the new small-signal current introduced by \(s_m\) as shown in Figure 4 (c), the new linearized small-signal DAE becomes

\[
G \cdot \delta v_n + C \cdot \delta v_n + E_i \cdot \delta j_i + E_i \cdot \delta j_i + 5. \delta s_m = -\mathcal{F}(X_0, \dot{X}_0, t);
\]

\[
E_v^i \cdot \delta v_n = 0; \quad E_v^i \cdot \delta v_n = 0;
\]

\[
\mathcal{K}_v^F \cdot \delta v_n + \mathcal{K}_s^F \cdot \delta s_m + \mathcal{K}_v^G \cdot \delta v_n + \mathcal{K}_s^G \cdot \delta s_m = 0.
\]

(11)

Therefore, we have the following matrix form for linearized system equation with all Jacobian matrices \((G, C, f, \mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G, \mathcal{K}_s^G)\) and incident matrices \((E_i, E_v^i, E_v^i, E_v^i)\):

\[
\begin{bmatrix}
G & E_i & E_i & \delta v_n \\
-E_v^i & 0 & 0 & 0 \\
\mathcal{K}_v^G & 0 & \mathcal{K}_v^F & \delta s_m \\
-\mathcal{K}_v^F & 0 & \mathcal{K}_v^F & \delta s_m
\end{bmatrix}
\begin{bmatrix}
\delta v_n \\
\delta j_i \\
\delta s_m \\
\delta s_m
\end{bmatrix}
+ \begin{bmatrix}
0 & 0 & 0 & 1 \\
0 & 0 & L_i & 0 \\
0 & 0 & \mathcal{K}_v^G & 0 \\
0 & 0 & \mathcal{K}_v^F & 0
\end{bmatrix}
\begin{bmatrix}
\delta j_i \\
\delta j_i \\
\delta j_i \\
\delta j_i
\end{bmatrix}
= -\mathcal{F}(X_0, \dot{X}_0, t).
\]

(12)

Note that both large-signal and small-signal system equations can be obtained when introducing internal state variables. Its implementation for STT-MTJ devices is shown in the following section.

B. Application of New MNA for STT-MTJ

As we have identified in the last section, a linearized system equation (12) has to be found to include STT-MTJ device into simulation with internal state variables. First we can generate the new state variable vector \(X = [v_n, j_i, j_i, s_m, \theta_m, \phi_m]^T\). Then we need to obtain the Jacobian terms \(G, C, \mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G, \mathcal{K}_s^G\) and \(S\) in (12). Note that there is no charge conservation in STT-MTJ, so \(C\) term is zero.

Applying equations (9) and (10) derived in last section to the STT-MTJ dynamic functions described in (1), (2), (5) and (6), we can easily obtain the Jacobian terms required as following:

\[
G = \begin{bmatrix}
\frac{d j_i}{dv_n} & -\frac{d j_i}{dv_n} \\
-\frac{d j_i}{dv_n} & \frac{d j_i}{dv_n}
\end{bmatrix};
\]

\[
S = \begin{bmatrix}
v_n \times \frac{d G}{d \theta_m} & 0 \\
-v_n \times \frac{d G}{d \theta_m} & 0
\end{bmatrix};
\]

\[
\mathcal{K}_v^F = \begin{bmatrix}
-\frac{d f(\phi_m, j_i)}{dv_n} & \frac{d j_i}{dv_n} & \frac{d j_i}{dv_n} & \frac{d j_i}{dv_n} \\
\frac{d j_i}{dv_n} & \frac{d j_i}{dv_n} & \frac{d j_i}{dv_n} & \frac{d j_i}{dv_n}
\end{bmatrix};
\]

\[
\mathcal{K}_v^G = \begin{bmatrix}
\frac{d f(\phi_m, j_i)}{dv_n} & \frac{d j_i}{dv_n} \\
0 & \frac{d j_i}{dv_n}
\end{bmatrix};
\]

\[
\mathcal{K}_s^G = \begin{bmatrix}
0 & 0 & 0 & 0
\end{bmatrix};
\]

where \(\frac{d j_i}{dv_n}\) and \(\frac{d j_i}{dv_n}\) can be derived from equations (1) and (2) and \(\frac{d j_i}{dv_n}\), \(\frac{d j_i}{dv_n}\) and \(\frac{d j_i}{dv_n}\) can be derived from equations (5) and (6), respectively.

In addition, note that \(G\) is conductance of STT-MTJ; \(S\) is memductance of STT-MTJ; \(f(\phi_m, j_i)\) is the function at the right hand side of equation (5). Recall that \(\omega_m\) is the angular movement speed of \(\phi_m\) defined in TABLE II. As such, all the Jacobian terms required for linearized system equation (12) are established, with which STT-MTJ device simulation considering internal state variables can be implemented in the SPICE-like simulator accordingly.
IV. NUMERICAL EXPERIMENT AND DISCUSSION

The transient simulator is implemented in MATLAB with modern data structure of SPICE to consider both STT-MTJ and CMOS devices. With the use of the newly developed SPICE-like simulator considering the internal state variables of STT-MTJ devices, a number of numeric experiments are conducted for designs of hybrid CMOS and STT-MTJ memory circuits. Other than the accurate dynamic models of STT-MTJ and CMOS devices, it also contains the basic circuit elements such as BJT, capacitor, resistor and voltage/current source. All numerical experiments are conducted on the same work station with Intel Core i5 CPU and 8G RAM.

A. Verification of Dynamic STT-MTJ Model with Internal State Variables

In order to validate our STT-MTJ model, the device-level simulation results are compared to the experiment verified modeling results shown in [9] with the same device parameters. The area of STT-MTJ cross-section is 130 × 90 nm², and the thickness of free layer is 2 nm. The saturation magnetization is 1000 emu/cm², and the crystal anisotropy is 200e. The polarization efficiency is 0.57 with tunnel magneto resistance (TMR) around 100%. The damping parameter is 0.005. 500 Ω is assigned as the GMR at P state ($R_P$). The voltage-dependent tunneling conductance coefficient for P and AP state are set to 0.1 and 0.65 to fit the TMR voltage relationship. The same STT-MTJ model is used for the following experiments for consistency.

Figure 5 shows the free-layer switching time versus STT-MTJ driving current. We can see that our model fits well with the results reported from [9]. Moreover, we can see the switching time increases very fast when the driving current approaches the critical current. In addition, a huge current has to be applied when a very short switching time is required.

![Figure 5. STT-MTJ device simulation result: switching time versus driving current, which is consistent to the reported results in [9].](image)

Under constant current driving condition, the dynamic behaviors can be observed from Figure 6, which shows the changes from resistance, voltage and two internal state variables (θ and ϕ) of STT-MTJ. A typical resistance fluctuation of STT-MTJ during state transition [10] is demonstrated. The STT-MTJ is initially at P state which has a smaller GMR ($R_P$). Upon applying a 600μA driving current, it is switched to AP state in about 10ns. ϕ increases continuously with a very high speed according to the large gyromagnetic ratio. θ starts to deviate from the original value once the current is applied. Its maximum deviation increases exponentially with time before the reversal happens. Under the constant current condition, the voltage changes with the STT-MTJ resistance simultaneously, of which the fluctuation is observable after 5ns and jumps to 850Ω at 10ns. This fluctuation decays very fast after reversal, and then STT-MTJ enters into the other stable state. Note that these dynamic behaviors of resistance fluctuation cannot be observed under the equivalent circuit based STT-MTJ model in [8].

B. Hybrid simulation with CMOS for NVM Application

We further investigate the STT-MTJ dynamic behavior in the design of non-volatile memory. A typical hybrid CMOS-STT-MTJ MRAM cell is shown in Figure 8(a). In the “write-1”-operation, WL is connected to VDD, and BL and SL are connected to VDD and GND, respectively. In the “write-0”-operation shown in Figure 8(b), the polarities of SL and BL line are interchanged. NMOS is included to simulate the actual operation of STT-MTJ based memory cell. Here we choose VDD to be 1.2V as a common biasing for 65nm process. The dynamic model of STT-MTJ with NMOS is compared with the static model driving by constant current in the switching time of “write-1” operation. Note that the switching time with static model can also be obtained from Equation (3). From the simulation results shown in Figure 7, we can see that the switching time obtained by the static model with constant current [7] is over estimated for the changing process: AP to P, and is also under estimated for the changing process: P to AP. This is because the actual driving condition of STT-MTJ in NVM application is constant voltage instead of constant current. We can also observe that the actual switching time of “write-1”-operation is 3X smaller than that of the “write-0”-operation. As such, the writing-pulse-width for 0 and 1 is not necessarily to be the same. Moreover, because the voltage is more than 1V across the STT-MTJ device, the resistance stays at 550Ω after reversal from P to AP, and it will return to 1000Ω once the applied voltage is removed.

![Figure 6. Dynamic responses of STT-MTJ resistance and state variables under the step-constant-current induction.](image)

C. Runtime Scalability Study

We further evaluate the circuit-level simulation efficiency of our developed simulator for STT-MTJ model with internal state variable. The runtime scalability study is performed on a size (bit) scalable memory design. One example of 16-bit memory is shown in Figure 8 (c). In order to make the comparison, the equivalent circuit of STT-MTJ given in [8] is also created in our SPICE-like simulator. And the transient simulations are performed for both approaches (Memductance with internal
state variable and equivalent circuit) for 10 time steps. The runtime simulation results are shown in Figure 9. For a 4-bit memory simulation, the CPU time of our internal state variable based simulation is only half of equivalent circuit based approach. With the increasing size of memory, the netlist complexity of equivalent circuit approach grows much faster than our approach. Therefore, the time reduction keeps increasing with the size of memory. For a 512-bit memory, the CPU time of internal state variable based simulation is more than 20 times smaller than the equivalent circuit based simulation.

Figure 7. Comparison between the dynamic model and static model: (a) under write-0 and (b) under write-1.

Figure 8. Circuit diagrams of STT-MTJ memory cell: (a) simplified memory cell for write-1; (b) simplified memory cell for write-0; and (c) 16-bit STT-MTJ MRAM with 4 bit-lines and 4 word-lines.

V. CONCLUSION

Internal state variables have been identified for STT-MTJ to consider the dynamic behavior. The according modified nodal analysis considering internal state variables is developed inside one SPICE-like simulator to provide efficient transient simulation. The experiment results show that our proposed method is more suitable for large scale hybrid CMOS and STT-MTJ devices than the equivalent circuit approach from two aspects. Firstly, it can simulate the dynamic behavior of STT-MTJ under arbitrary driving condition while the equivalent circuit approaches can only be used at constant current driving condition. Secondly, compared to the equivalent circuit approaches, the simulation time is reduced by 20 times by our proposed method for large memory circuits.

Figure 9. CPU runtime comparison between our internal state variable method and the equivalent circuit based model [8].

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REFERENCES


