Testability-analysis driven test-generation of analogue cores

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Abstract

A new definition of the testability transfer factor for circuit components that provides better sensitivity with respect to parametric deviations is presented. New equations for the testability measures in a mixed-signal core are given. Testability analysis is used for test-pattern generation and for consideration of inserting wrapper cells. The simulation results show the effectiveness of the approach.

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1. Introduction

Systems-on-Chip (SoC) have become increasingly prevalent in the semiconductor industry. To gain a competitive advantage in today’s demanding electronics market, system designers try continually to add new functionality, increase performance, and reduce costs in each new development cycle. This trend of integration and core-based design is presenting a new challenge for testing. In such complex systems an efficient method for analogue test generation is required. In order to reduce simulation time, we have used testability analysis for test-pattern generation.

The testability of nodes in a core is directly related to their controllability and observability. The controllability of a node in a circuit represents the ease of applying an arbitrary signal value at that node by full control of the primary inputs. The observability of a node represents the ease of determining whether or not the expected signal value occurs at the node by observing the signal values at the primary outputs of the circuit. The proposed equations for the Testability transfer factor (TTF) of a component (e.g. transistor, resistor, capacitor, etc.) in Ref. [1] give a low sensitivity of the TTF on variation of the component, especially for low impedances. Additionally, the derived test patterns are very complex for practical implementation.

A multi-frequency test generation technique for detecting faults using testability analysis has been developed to generate test signals for stand-alone analogue embedded cores under test. In this method, the testability analysis is performed for the fault-free circuit and for all possible faults from the fault list and the test patterns are generated subsequently. In order to verify the effectiveness of the method a locally designed electronic system is used. Since the input of an embedded core can be accessible from the primary SoC inputs via preceding blocks or by using wrapper cell structures, the testability analysis is used for consideration of inserting the wrapper cells.

2. Testability analysis

TTF of components are discussed in Refs. [1–3]. However, the proposed TTF equations give a low sensitivity of the TTF on variation of the components, especially for low impedances. Furthermore, the deviation of the TTF caused by deviation of the component impedance is proportional to the value of the component impedance [4]. This makes the analysis of process variations almost impossible. Additionally, the derived test patterns are very complex for practical implementation by signal generators.
A new definition of the testability transfer factor of a frequency dependent impedance $Z(\omega)$ is now presented to increase the sensitivity for low impedances:

$$\text{TTF}(Z(\omega)) = (1 - \log_{\text{OC}} |Z(\omega)|^a)^p$$  \hspace{1cm} (1)

An open circuit (OC) is modeled with a 10 MΩ resistance. The parameter $a$ provides an additional possibility to increase (decrease) the sensitivity of the TTF for low (high) values of impedance $Z(\omega)$. A once chosen value of the parameter $a$ cannot be changed during analysis. By using Eq. (1), the deviation of the component value will be transformed in the deviation of the TTF for that component. For example, for $a = 1$, the deviation of the testability transfer factor of a component is approximately one order of magnitude less than the deviation of the component. As one illustration of the achieved improvement by using our new definition for the TTF is that deviation of the previous defined TTF is close to directly proportional dependence of the value of the impedance; for an impedance $Z(\omega)$ with a nominal value of the 1 kΩ deviation of the TTF is four orders of magnitude lower than the deviation of the value of the component.

Using this approach, any circuit can be described with a signal flow graph (SFG). For further analysis, the SFG of a circuit with $n$ nodes will be described by a matrix $A(n, n)$, where $A(i, j)$ has a value equivalent to the TTF fan-in from node $j$ to node $i$. From Eq. (1) one can derive:

$Z(\omega) = \text{OC}^{1 - \text{TTF}(Z(\omega))^a}$ \hspace{1cm} (2)

From the equation for the equivalent impedance of parallel-connected impedances and Eq. (2), a value TTF\text{eq} for an equivalent TTF (parallel connection of $n$ fan-in/outs), can be constructed:

$$\text{TTF}_{\text{eq}} = \left(1 + \log_{\text{OC}} \sum_{i=1}^{n} \text{OC}^{(\text{TTF}^a)^{i_1}}\right)^a$$ \hspace{1cm} (3)

If the contribution of node $j$, with controllability $C_j$, to the controllability of node $i$ is defined as $A(i, j) * C_j$, then the values for controllability ($C_i$), observability ($O_i$) and testability ($T_i$) for node $i$ can be found by using the following Eqs. (4)–(6):

$$C_i = \left(1 + \log_{\text{OC}} \sum_{j \neq i} \text{OC}^{(A(i, j) * C_j)^a_{i_1}} - 1\right)^a$$ \hspace{1cm} (4)

$$O_i = \left(1 + \log_{\text{OC}} \sum \text{OC}^{(O(i, j) * A_j)^a_{i_1}} - 1\right)^a$$ \hspace{1cm} (5)

$$T_i = \sqrt{C_i * O_j}, \hspace{1cm} i = 1, \ldots, n$$ \hspace{1cm} (6)

The measures for all three properties of nodes are normalized to range between 0.0 (minimum) and 1.0 (maximum). Systems of nonlinear Eqs. (4) and (5) can be solved using the Newton–Raphson method. In order to speed up CPU time, the method is modified in such way that the matrix of the partial derivates (Jacobian) is found directly. The values for the controllability of the primary inputs and the observability of the primary outputs are 1.0 by default. For that reason, the values for the testability of the primary inputs and the testability of the primary outputs are only dependent on the observability and the controllability of the nodes respectively.

The obtained values for the testability of nodes are associated with the primary input and primary output. For circuits with multiple inputs/outputs one input node has to be chosen as primary input, and one output node has to be chosen as primary output. Finally, the testability of a node will be the maximum obtained value for the testability of that node for all possible choices.

3. Example circuit

An audio application, presented in Fig. 1, is used as an example to explore the analogue core-based testing. It is part of a locally designed system and includes a preamplifier, a fully embedded continuous time filter [5] and a voltage-current converter (VIC). The signal from the band-pass output (out_BP) of the filter is propagated to the VIC. The considered core for the test-pattern generation is the filter.

Based on the Tow–Thomas topology [6], the filter is consisting of four operational transconductance amplifiers (OTAs) and integrated capacitors, as shown in Fig. 2. In order to reduce harmonic distortion, the filter is implemented with fully differential inputs and outputs in 0.8 μm AMS CMOS technology. The filter core has two control variables: a short range tuning variable given by...
a $V_g$ voltage, and a large range programming variable, given by an $I_b$ biasing current. The transistor schematic of the OTA is presented in Fig. 3. The bias current of all OTAs in the filter is set to 200 nA and it defines the output frequency characteristic. The center frequency $f_c$ of the band-pass output is set on 13.4 kHz and the bandwidth is 12.4 kHz.

4. Test-pattern generation

Our formulation of the testability-transfer factor for a circuit component is dependent on the frequency. Hence, our testability analysis can only be used as a guide for the test generation of test signals with the frequency as the single associated test parameter. As a result of this boundary condition, each test signal will be described as a single sine-wave or multi-frequency signal.

Based on testability analysis, a simulator has been developed. The core is described with a SPICE netlist and a list of primary input/output nodes. The testability analysis is performed and the testability of each node in the core is calculated for the complete frequency range, using eight points per decade and 5 Hz for the start frequency.

The fault list consists of two types of faults: bridging faults between nodes and interconnection faults modeled as serial resistances. Next, the testability of a faulty circuit for all possible faults from the fault list is calculated and test-pattern generation is carried out. An error function is defined as the difference between the testability for the faulty and the fault-free case of the node where the fault occurred. If the error function for a frequency is under a predefined threshold, than that test signal frequency can be used for detecting that fault in the circuit.

A list of nodes with the lowest testability for the fault-free case and associated values for testability are listed in Table 1.

As seen from Table 1, node NET11 in the amplifier OTA1 is the node with the lowest testability. A bridging fault on that node can be considered as a worst-case bridging fault. In that case the band-pass output (out_BP) is considered as primary output and a bridging fault $R_b$ is inserted as depicted in Fig. 3.

The testability analysis is performed for the faulty circuit and the error function is calculated. For the detection of the fault, the next two frequencies can be used: $f_1 = 13.3$ kHz and $f_2 = 17.7$ kHz. For the test stimuli, a multi-frequency signal is generated from two sine waves with frequencies $f_1$ and $f_2$. According to specification of the filter, the DC offset of the test signal is set to 1.3 V, equal to value of the $V_{ref}$, and a magnitude of the 50 mV is calculated for both. The presented measurement results show that the proposed test stimulus can be easily generated using an Arbitrary Waveform Generator and used for detection of faults as can be seen in Fig. 4a.

Simulation results for the test output for the fault-free and faulty case for a bridging fault from the fault list as response to the test stimulus are presented in Fig. 4b.
By using testability analysis, a reduction in CPU time by a factor 11 has been achieved, compared with required CPU time for the AC simulation using the simulator HSPICE.

5. Embedded situation

In the embedded situation, inputs as well as outputs of the filter core are accessible via wrapper cells similar as suggested within IEEE proposed standard P1500 [7] like the DfT circuitry that have been proposed in [8]. An embedded core can be tested by providing test stimuli to the core and observing test responses of the core by using wrapper cells or by propagating signals through preceding and succeeding cores [9]. The considered part of the SoC is presented in Fig. 5. Analog test buses are denoted Ab1 and Ab2 and their test pins are indicated with AT1 and AT2. Scan chain input and scan chain output are represented with SI and SO, while TBIC and WIR are test bus interface circuit and wrapper instruction register, respectively.

In order to consider the insertion of the wrapper cells it is assumed that we have full observability of the filter output. The testability analysis is performed for the preamplifier core and the filter core together, and the requirement of the wrapper cells between them is considered.

If the testability of all nodes in both cores is adequate to be tested via primary inputs (PI+ and PI-) there is no need for the wrapper cells on the filter inputs. In that way, it is possible to reduce the number of the wrapper cells and decrease the DfT circuitry.

An experiment has been carried out with out_LP+ node in the filter, as node with the lowest testability. A bridging fault is inserted between that node and the NET38 node in the OTA3. Fig. 6 shows the signature for the fault-free and faulty circuit for the bridging fault. The required input signal to detect the fault is a multi-frequency signal generated from two sine waves with frequencies f1 = 15.8 kHz and f2 = 20.5 kHz. The data shows the faulty behavior and the dashed lines represent the signal resulting from the faulty circuit. As one can see in the figure, there is a clear distinction between the two. This difference is sufficient to detect the fault, in the presence of accepted tolerances.

The presented results show substantial difference between signals observed on the filters output for faulty and fault-free case. The preamplifier core and the filter core can be tested by providing a test signal to the preamplifier core and observing the signature at the output of the filter core. There is no need for a wrapper cell between the two circuits.

6. Conclusions

New definitions for the TTF and new equations for testability measures have been introduced. For test-pattern generation for stand-alone cores the testability analysis has been presented. A possibility of using testability analysis for consideration of the insertion of wrapper cells in a SoC is presented also.

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References


