Concurrent Chip-Package Design for 10GHz Global Clock Distribution Network

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Abstract
As a result of the continuous downscaling of the CMOS technology, on chip frequency for high performance microprocessor will soon arrive 10GHz according to international technology roadmap for semiconductors (ITRS). In this paper, a 10GHz global clock distribution network using standing wave approach was analyzed on chip and package level. On chip level, a 10GHz standing wave oscillator (SWO) for global clock distribution network using 0.18um, 1P6M CMOS technology, is designed and analyzed. The simulation results show that the skew is well controlled (about 1ps) while the clock frequency variation is about 20% because power/ground return paths exist in different metal layers. On package level, we assume that the chip size is 20mm*20mm and flip-chip bonding technology is used. The simulation results show that the skew at random positions of the transmission line (spiral or serpentine shape) is within 10% of \( \tau_{\text{clk}} \) when the attenuation is about 1.5dB. For attenuation from 1.5dB to 6.7dB, the peak positions \((n\times\lambda/2)\) can be used as clock node. For the mesh and plane shape, the skew is controlled within 10% of \( \tau_{\text{clk}} \) using standing wave method.

1. Introduction

As CMOS technology advances into nanometer feature size, on chip frequency for high performance microprocessor will soon arrive 10GHz [6]. With gigahertz frequencies, using copper and wider wires, long interconnects such as clock, bus and power/ground lines exhibit transmission line behavior [2, 3, 4]. Delay and signal integrity are becoming major concerns in integrated circuit design while on-chip global clock distribution has become an increasingly tough task because of skew and jitter of the clock network. Besides traditional H-tree clock distribution network, standing wave approaches [8, 9] are becoming a potential solution for global clock distribution. In addition to be treated as parasitic components, interconnects can also be used as useful devices [1] for standing wave oscillator (SWO) design. So an accurate model of the interconnect must be extracted. Three different models of on-chip interconnects are usually used in VLSI design [5]:

- RC model, this model doesn’t include inductance. The model is less accurate but is widely used in state-of-the-art VLSI design.
- RLC model, the model consists of distributed LRC networks.

In this paper, the SWO circuit performance is followed by package level global clock distribution. In the following text, we first describe interconnect model and extraction. Then SWO circuit design for global clock distribution is described. This is followed by package level global clock distribution description. Finally, conclusions are made.

2. Interconnect model and extraction

Central to the design and analysis of interconnects is electromagnetic (EM) field solvers. The EM solvers use the geometry information to solve the Maxell’s equation by numerical methods. Currently, a number of EM simulators are used including full 3D, 2.5D and 2D solver (HFSS from Ansoft, Momentum from Agilent) to obtain S-parameters. Correct usage of these tools (boundaries, complexity of the structure, tradeoffs between accuracy and computer cost) is of
paramount importance to capture the important physical effects within reasonable simulation time and memory usage. There are three types of transmission line architecture, namely microstrip line, coplanar line and stripline. In order to obtain parameters of interconnect, we first use HFSS as the field solver (3D) to obtain S-parameters, and then distributed network elements \( R, L, G \) and \( C \) are extracted.

For interconnects the model has been developed that presents, in the frequency domain, the interconnect voltage and current in terms of propagation constant \( \gamma \) and characteristic impedance \( Z \). The propagation constant \( \gamma \) and characteristic impedance \( Z \) are described by four distribution network elements \( R, L, G \) and \( C \). The infinitely small subsection of this model incorporating distributed network is shown in Fig.1.

From [7], the relationships between S-parameter, propagation constant \( \gamma \) and characteristic impedance \( Z \) are:

\[
\begin{align*}
S_{11} & = \frac{1 - \gamma^2}{\gamma^2 + K} \\
S_{21} & = \frac{Z_0}{\gamma} (1 - \gamma^2)^{-1/2} \\
Z & = \left( \frac{Z_0}{\gamma^2} \right)^{1/2} \\
K & = \left( \frac{2S_{11} - (S_{11}Z_0^2 + 1)^{1/2}}{Z_0^2(2S_{21})^2} \right)^{1/2}
\end{align*}
\]

Once the propagation constant \( \gamma \) and characteristic impedance \( Z \) are determined, from standard transmission line relationships:

\[
\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta
\]

\[
Z = \frac{R + j\omega L}{\sqrt{G + j\omega C}}
\]

Then \( R = \text{Re}(\gamma Z) \), \( L = \text{Im}(\gamma Z)/\omega \), \( G = \text{Re}(\gamma/Z) \) and \( C = \text{Im}(\gamma/Z)/\omega \) (5)

Thus the transmission line parameters are determined by equation (1- 5).

3. On-chip global clock analysis using SWO
3.1. Interconnect analysis for SWO

One coupled on-chip microstrip transmission line (TL) should be optimally designed for SWO circuit. In this paper, we use 1.8V, 0.18um, 1P6M CMOS technology. The insulator is oxide and its dielectric constant is 4. The technology parameters for metal layers are shown in Table 1. The heights from metal 6 (M6) to different metal layers are: M1=6.52um, M2=5.14um, M3=3.76um, M4=2.38um, M5=1um. The parameters of the coupled microstrip line are as follows: width= w um, space= s um, height= h um.

### Table 1. Technology parameters for metal layers

<table>
<thead>
<tr>
<th>Thickness (um)</th>
<th>Min. width (um)</th>
<th>Min. space (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal 6</td>
<td>2.34</td>
<td>1.5</td>
</tr>
<tr>
<td>Metal 5-1</td>
<td>0.53</td>
<td>0.28</td>
</tr>
</tbody>
</table>

Fig.2 PUL resistance and inductance for various heights of the microstrip line

For the microstrip line, we assume two signal wires running on the top metal layer (M6) because it has lowest resistance. The ground layer is composed from one of the other metal layers. The parameters of microstrip line are as

Fig.3 PUL attenuation for various heights of the microstrip line
follows: \( w=14\,\text{um} \) and \( s=4\,\text{um} \). The PUL R, L, attenuation and C for various heights are shown in Fig.2, Fig.3 and Table 2, respectively. In Fig.2, for \( h=1\,\text{um} \), the resistance increases by 62\% from DC to 10GHz while the inductance decreases by 16.7\%. When the height of microstrip line is changed from 6.52\,\text{um} \) to 1\,\text{um}, the loop inductance decreases by 21.9\% in 10GHz and the capacitance increases by 271\%. Consequently the attenuation increases by 277\%. So metal 1 should be used as the ground layer because of less attenuation.

In Fig.4, the microstrip line parameters are \( h=6.52\,\text{um} \) and \( s=4\,\text{um} \). Attenuation is plotted for metal width from 4\,\text{um} \) to 60\,\text{um} \). Optimal width is found for each frequency and for 10GHz this is 14\,\text{um} \). Based on this result we use this width in our design.

### Table 2. PUL capacitance for various \( h (w=14\,\text{um}, s=4\,\text{um}) \)

<table>
<thead>
<tr>
<th>( h ) (\text{um})</th>
<th>6.52</th>
<th>3.76</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_s ) (\text{F/m})</td>
<td>1.152e-10</td>
<td>1.806e-10</td>
<td>4.283e-10</td>
</tr>
</tbody>
</table>

In real chip design, parallel or orthogonal power/ground wires may exist around the microstrip line. They may act as current return paths and hence they can greatly change the parameters of interconnects. In our analysis cases, case1 means there is only one coupled TL (\( w=14\,\text{um}, s=4\,\text{um} \) and \( h=6.52\,\text{um} \)) and its return path is metal 1. For caseB_1, there are two parallel ground wires one on each side of the TL on the same layer, \( w=s=4\,\text{um} \). For caseB_2, there are four parallel ground wires on the same layer. The results are shown in Fig.5. At low frequencies return currents seek the path of least resistance, and hence the return currents are carried primarily on total return paths because of their greater combined cross-section, and hence greater combined conductivity. Thus at low frequencies, resistance for caseB_2 is 27\% smaller than caseB_1. The inductance for caseB_2 increases by 6\% compared with caseB_1 because the current makes a larger loop. At high frequencies, currents redistribute to minimize the loop inductance. The closest ground return wires become important when their close proximity to the signal conductor becomes an important factor in minimizing total loop inductance. So the inductances for caseB_2 and caseB_1 have almost the same value.

Fig.5 PUL inductance and resistance of microstrip line when parallel ground lines exist in the same layer (metal layer 6)

<table>
<thead>
<tr>
<th>( h ) (\text{um})</th>
<th>6.52</th>
<th>3.76</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_s ) (\text{F/m})</td>
<td>1.152e-10</td>
<td>1.806e-10</td>
<td>4.283e-10</td>
</tr>
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</table>

Two types of orthogonal lines exist in metal layer 5. For caseC_1, the line width equals to \( 4\,\text{um} \) and space equals to
16um. For case C_2, the line width is same while the space equals to 4um. The simulation results are shown in Fig.6. The PUL inductance and resistance are almost same in case1, caseC_1 and caseC_2, while the capacitances are 1.152e-10F/m, 2.51e-10F/m and 3.16e-10F/m, respectively. This leads to low characteristic TL impedance and hence it increases TL attenuation.

Two types of parallel ground lines exist in metal layer 4. For caseD_1, w= 4um and s=16um and for caseD_2, w=4um while s= 4um. The simulation results are shown in Fig.7. This architecture decreases the loop inductance and increases the capacitance of the line. Hence it further increases the attenuation of the TL line.

3.2. SWO for global clock distribution

The design of global clock distribution for a multi gigahertz microprocessor has become an increasingly difficult and time-consuming task. A global clock network that uses a standing wave oscillator has the potential to significantly reduce both skew and jitter [8, 9]. We use the topology similar to [8] to show how interconnects in a real chip will affect the performance of SWO such as frequency and skew. The SWO architecture is shown in Fig.8. The cross-couple pairs, which act as negative resistors, are used to compensate the loss of the transmission line in order to reduce the residual traveling wave.

\[
\alpha(\omega_{osc})<0, L = \frac{\pi}{\beta(\omega_{osc})}
\]

where
\[
\alpha = \text{Re}(\gamma) = \text{Re}\left(\sqrt{R + j\omega L + Gd + j\omega C}\right) = \frac{R}{2Z_0} - \frac{GdZ_0}{2}
\]
\[\beta = \text{Im}(\gamma)\]
L is the length of the transmission line

Table 3 shows the parameters for SWO simulation. The parameters are obtained at 10GHz. For SWO, the size of the MOS transistor is 50um/0.18um and the length of TL is 5.328mm. The number of cross-couple stages is 5. The total current is 4.2mA and power consumption is 7.5mW. The simulation waveform (case1) is shown in Fig.9. The results show that the skew in different positions is within 1ps. For various cases, the skew is well controlled (1ps), but frequency variation arrives 20%, as shown in Table 4. So, in real circuit designs, interconnect should be accurately predicted. For example, the dense orthogonal lines such as in caseC_2 should be avoided. On the other hand, robust circuits should be adopted to tolerate the parameter variations of the interconnect. For example, a tunable SWO should be used in standing wave clock distribution.

4. Package level global clock distribution

The board-level standing-wave clock distribution described in [11] is a straightforward but effective way of generating a standing wave that has potential applications for package-level clock distributions, as shown in Fig.10. The clock is driven by a sinusoidal clock buffer and the terminator is opened reflecting completely the clock back to the driver. The superposition of the incident and reflected waves forms a standing wave. In this paper, we assume that the chip size is 20mm*20mm. Flip-chip bonding technology and MCM-L technology are used. The parameters are: substrate is low loss Rogers 4003, which has \(\varepsilon_r=3.38\) and loss tangent =0.0027 at 10GHz. The min. pitch of solder bump is 200um; height is 50um, and diameter is 70um. Other parameters of wire are shown in Table5.
The clock network in substrate can be spiral, serpentine, mesh and plane, as shown in Fig.11. We first explore spiral or serpentine shapes. The parameters of the microstrip line are: width=100um, thickness=35um and height = 100um. The attenuation is about 12.3dB/m at 10GHz. The extracted PUL parameters are: R=0.1605 ohm/mm, L=0.3535nH/mm and C=0.0841pF/mm. A 10GHz voltage controlled LC-oscillator (VCO) which has a tuning ranges of 29% [13] is used. The half-wave-length of the TL is 8.98mm in an ideal case (assuming that we only consider TL itself and don’t consider the parasitic of the solder bump and the clock load capacitance). Because the frequency is 10GHz, the TL loss cannot be neglected. So there is a traveling wave which exists in the TL. Hence, it will increase the skew of the clock. With continuously increasing the length of TL, the phase in different position varies very much. But in some special points (peaks of voltage amplitude), there is almost no phase difference. In our simulation results, the skew in random positions of the TL will be larger than 10% of $\tau_{ck}$ when the TL length is larger than $5\lambda$. However, at peak positions ($n^{*}\lambda/2$), the skew is kept within 10% of $\tau_{ck}$ for TL lengths up to $30\lambda$ (about 0.5m).

We can conclude that when the attenuation of the TL is within 1.5dB, we can choose a random position of TL as the clock node. For attenuations from 1.5dB to 6.7dB, the peak positions should be chosen as the clock node. This is shown in Fig. 12 when the attenuation is 6.7dB. These clock nodes can directly connect to the local clock distribution network of the chip.

Table 5. Line parameters in MCM_L technology

<table>
<thead>
<tr>
<th>Min. line Space</th>
<th>Min. line Thickness</th>
<th>Min. substrate Thickness</th>
<th>Min. line Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>75um</td>
<td>5um</td>
<td>100 um</td>
<td>75 um</td>
</tr>
</tbody>
</table>

![Fig.10. Global clock network on package level](image)

![Fig.11. Various clock network shapes on package](image)

![Fig.12. Waveform for peak position ($n^{*}\lambda/2$) at TL when the attenuation is 6.7dB](image)

![Fig.13. Meshes of clock plane and its modeling](image)

The same microstrip line structure is used to make a mesh. The clock is 10GHz and its wavelength is about 18mm. The total width is 20mm and mesh pitch is 1mm. The lumped model (one section RLC) is used to represent each mesh edge. The parameters of TL are the same as spiral shape. In different positions the skew is about 8ps. In this case again we don’t consider the parasitics of the solder bump and input capacitance of the clock buffer.

![Fig.14. Waveform for random positions on plane shape](image)

The clock plane can be simulated by an equivalent circuit of a mesh of transmission line mode [12]. Fig.13 shows that the clock plane is divided into many meshes and each cell can be represented by 4 short transmission lines. When the size of the mesh is small enough compared to the wavelength of the operating frequency, each mesh can be modeled as a lumped L, R, and C network. The chip size is 20mm*20mm. So we divide the plane into 20 meshes. The parameters of each short
transmission line are: R=0.043ohm/mm, L=0.0915nH/mm and C=0.4167pF/mm. The simulation result is shown in Fig.14. In different positions, the skew is within 10% of $\tau_{clk}$.

5. Conclusions

In this paper, a 10GHz standing wave approach for global clock distribution is analyzed on chip and package levels. For on chip SWO, the simulation results show that the clock skew is well controlled (about 1ps) while the clock frequency variation is about 20% because of neighboring power/ground return paths exist in different metal levels. On package level, the mesh and plane shapes are suitable for the global clock network when the chip size is 20mm*20mm.

References

5. Li-Rong Zheng, Design, Analysis and Integration of Mixed-Signal Systems for Signal and Power Integrity. PH.D thesis, pp.54-p56, Royal Institute of Technology, ISSN 1104-8697