Suppression of Jitter Effects in A/D Converters through Sigma-Delta Sampling

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Abstract

This paper describes a new sampling circuit topology that shapes clock jitter induced sampling noise in much the same way a \( \Sigma \Delta \) Analog-to-Digital Converter (ADC) shapes quantization noise. The sampling circuit consists of a continuous-time (CT) integrator followed by two switches. One for the output and one for the feedback. Its intended use is as a front-end for ADCs where jitter is a concern, e.g. wideband or bandpass \( \Sigma \Delta \) ADCs. The main benefit of this converter is that its sampling noise due to jitter is, to a large extent, independent of the signal frequency. This means that as the signal frequency increases, and traditional sampling circuits’ performance deteriorates, the proposed \( \Sigma \Delta \) sampler offers a maintained high sampling accuracy.

Calculations and simulations in this paper show that the \( \Sigma \Delta \) sampler has higher performance than a traditional sampling circuit (circuit noise not included), if the main part of the signal power is in the upper portion of the frequency band. The maximum benefit, assuming the input is a single sinusoidal tone, is approximately 4.75 dB in signal-to-jitter-noise ratio (SJNR).

1 Introduction

In order to fully utilize the inherent superiority of digital signal processing (DSP) over analog signal processing it is necessary to digitize the analog signal as early as possible in a receiver path, thereby minimizing the number of “noise-adding” analog processing steps. Because of finite frequency space and the need for high data rates, modern applications often use carrier frequencies in the GHz range. However, state-of-the-art ADCs [7, 8] cannot sample and digitize the signal at this high rate with adequate accuracy. Therefore the signal is downconverted in one or more steps to an intermediate frequency (IF) usually in the MHz range and then digitized. Each downconversion is an analog processing step which means that the fewer and simpler such steps there are before digitization, the better the theoretical performance. In order for an ADC to have the chance of supplying a sufficiently accurate digital signal to the DSP, a number of issues have to be resolved. One of those, dominating at high signal and sampling frequencies, is clock jitter.

Clock jitter is one of the main obstacles when trying to design an ADC that can operate at high frequencies. Clock jitter is defined as a random (stochastic) fluctuation of timing on a clock. Since the clock edges determine at which time instants an analog signal is sampled, a random fluctuation in the timing of the clock edges will produce a non-uniformly sampled signal. If the real sampling instants deviate from the ideal (expected) sampling instants, the observed (sampled) signal will be a distorted version of its analog representation. An exaggerated example of this is shown in figure 1 where a sinusoidal signal with frequency \( f_{\text{sig}} = 1.125 \text{ MHz} \) has been sampled at a rate of \( f_s = 100 \text{ MHz} \) with clock jitter having standard deviation \( \sigma = \frac{1}{f_s} \).

The stochastic nature of clock jitter depends on several factors, e.g. clock source and dynamic changes (EM, temperature, power supply, etc.) in the operating environment. The clock source is commonly a crystal oscillator with very low phase noise (clock jitter viewed in frequency domain). However, crystal oscillators are very unflexible
when it comes to frequency choice. Therefore, a phase-locked-loop (PLL) is often used in order to upconvert the oscillator frequency. After upconversion, the different analog and digital circuit blocks in a system usually need more than a single phase time reference and therefore some sort of clock generation circuitry is needed. All of the operations on the oscillator clock introduce jitter and even if the circuit blocks of the PLL and clock generation were noiseless, EM noise coupled through the substrate and power supply would deteriorate the clock quality.

The jitter induced noise power through sampling is quadratically proportional to the signal frequency \([1]\). A high input signal frequency combined with successful shaping of quantization noise has resulted in that clock jitter is one of the dominant noise contributors in wideband and bandpass \(\Sigma\Delta\) ADCs. Therefore, it is natural to try to adopt what \(\Sigma\Delta\) modulators do with quantization noise to sampling noise. In some sense, this has already been done in the field of CT \(\Sigma\Delta\)s \([5]–[6]\) since jitter induced sampling errors are injected inside the noise shaping loop. However, traditional CT \(\Sigma\Delta\) ADCs do not benefit from jitter noise shaping since they have an additional, and dominant, jitter injection mechanism besides non-uniform sampling of the integral of the input signal. This mechanism comes from the non-uniform sampling of the integral of the DAC output, which typically has a rectangular or trapezoidal waveform. In recent years, however, a few researchers \([5]–[6]\) have explored ways to reduce this jitter injection mechanism through altering the DAC feedback waveform. The drawback in doing this is mainly that by making the DAC more complicated, more error sources are introduced that are not compensated for by the feedback loop. Furthermore, those solutions do not truly focus on the problem with jitter induced sampling noise that all ADCs share but rather try to circumvent a specific issue with CT \(\Sigma\Delta\) ADCs.

In this work we present a new sampler topology that shapes clock jitter induced noise away from the signal band thus allowing other ADCs (not just CT \(\Sigma\Delta\)s) to benefit from reduced clock jitter sensitivity.

2 \(\Sigma\Delta\) Sampling Circuit Topology

There are many ways to sample a signal and many sampling circuits exist in the literature. A very basic sampling circuit consists of two switches operated on a two phase clock and a capacitor \(C\) (see fig. 2 left). This sampler is used, in this work, as a performance comparison to the \(\Sigma\Delta\) sampling topology and is referred to as an ordinary or traditional sampler. The \(\Sigma\Delta\) sampler (see fig. 2 right) consists of an operational transconductance amplifier (OTA) or operational amplifier (OPAMP) connected as a CT integrator with \(R_1\) and \(C_1\), a capacitor \(C_2\) acting as charge supplier in the feedback path, and an output capacitor \(C_4\) providing the time-discretized voltage.

In a real design, all capacitors should be made of equal size. Here they are named with indices to allow for investigation of mismatch effects. The \(\Sigma\Delta\) sampler operates on a two-phase non-overlapping clock \(\{\phi_1, \phi_2\}\) with a duty cycle \(d_c\) and a period \(T = \frac{1}{d_c}\). The sampler works in much the same way as a CT \(\Sigma\Delta\) ADC without the ADC and DAC. The analog signal \(V_{in}(t)\) is continuously integrated onto \(C_1\) and being sampled onto \(C_2\) and \(C_3\) as \(\phi_1\) falls (assuming falling-edge triggered switches, e.g. NMOS). During \(\phi_2\) high, the voltage over \(C_3\) is fed to the output, which in turn may be connected to an ADC input, and the charge on \(C_2\) is fed back and subtracted from the charge on \(C_1\). In short, as the analysis will show, the output voltage is given by a difference between two consecutive samples:

\[
V_{out}[i] = V_{C1}\left(iT\right) = -\frac{1}{R_1C_1} \int_{t=(i-1)T}^{iT} V_{in}(t) dt
\]  

3 Performance Analysis

The following analysis is based on a constant switch resistance approach and an ideal amplifier. Furthermore, the analog input signal is assumed to be a single sinusoid \(V_{in}(t) = A\sin(\omega t)\). Let the different clock phases \(\phi_1\) and \(\phi_2\) be defined by their transition instants (starting low \(\rightarrow\) high):

\[
\phi_1 = \{t_1[1], t_2[1], \ldots, t_1[N], t_2[N]\} \\
\phi_2 = \{t_2[1], t_2[1], \ldots, t_2[N], t_2[N]\}
\]

Ideally, the time shift, or skew, between \(\phi_1\) and \(\phi_2\) is \(\frac{T}{2}\).

3.1 Input-output characteristic

State space equations are set up for the \(\Sigma\Delta\) sampler and solved analytically for the different phase state combinations (circuit configurations). As is the case with a \(\Sigma\Delta\) ADC, the \(\Sigma\Delta\) sampler has memory and its current state not only depends on the input signal but also on previous states.
However, since there is no quantizer and if we assume there is enough time for full settling, it is straightforward to obtain an exact non-recurrence relation in time-domain for the output voltage. To also illustrate mismatch effects we write the relation in the following way:

\[ V_{\text{out}}[i] = V_{\text{out}}^{\text{m-ideal}}[i] + V_{\text{out}}^{\text{mismatch}}[i] \]  

where the first term, free of mismatch non-idealities, is given by:

\[ V_{\text{out}}^{\text{m-ideal}}[i] \approx \frac{A}{\omega T_1} \left( \cos(\omega(t_1[i] - \tau_2)) - \cos(\omega(t_1[i] - 1 - \tau_2)) \right) , \quad i = 3, \ldots, N \]  

and the second term accounts for capacitor and switch resistance mismatches:

\[ V_{\text{out}}^{\text{mismatch}}[i] \approx -\frac{A}{\omega T_1} m_{C12} \left( \cos(\omega(t_1[i] - 1 - \tau_2)) + \cos(\omega(t_1[i] - 2 - \tau_2)) \right) + \frac{A \tau_2}{T_1} (m_{R23} + m_{C23}) \sin(\omega t_1[i]) , \quad i = 3, \ldots, N \]  

where

\[ m_{Cub} = C_b/C_a - 1 \quad \text{and} \quad m_{R23} = R_3/R_2 - 1 \]  

Equations (5) and (6) have been obtained assuming that \( \omega^2 \tau_2^2 \ll 1 \) for \( i = \{1, 2\} \). For \( i = \{1, 2\} \) the relations (5) and (6) are slightly different because of initial conditions. However, this does not matter much in a power analysis since it is a transient state and the relations (5) and (6) represent the steady state.

### 3.2 Clock Jitter Impact on Sampled Voltage

We define the jitter on each of the phases \( \phi_1 \) and \( \phi_2 \) as a deviation of their corresponding transition instants:

\[ t_1'[i] = (i - d_c) T + \gamma_1[i] \quad t_1'[i] = i T + \gamma_1[i] \]

\[ t_2'[i] = (i + 1/2 - d_c) T + \gamma_2[i] \quad t_2'[i] = (i + 1/2) T + \gamma_2[i] \]

Given sufficiently small jitter magnitudes \( \gamma_k[i] \), we may approximate the output voltage in the following, linearized, way

\[ V_{\text{out}}[i] \approx V_{\text{out}}^{\text{j-ideal}}[i] + V_{\text{out}}^{\text{jitter}}[i] \]  

where

\[ V_{\text{out}}^{\text{j-ideal}}[i] = T \left\{ V_{\text{out}}^{\text{m-ideal}}[i] + V_{\text{out}}^{\text{mismatch}}[i] \right\} \]

\( T \{ \cdot \} \) is a time-transformation where all \( t_1'[j] \) in (5) and (6) are replaced with \( j T \). \( V_{\text{out}}^{\text{jitter}}[i] \) in (8) is the sampling error, or noise, caused by clock jitter and is given by

\[ V_{\text{out}}^{\text{jitter}}[i] \approx \frac{A}{\tau_1} \left[ \gamma_1[i] \sin(\omega(i T - \tau_2)) - \gamma_1[i - 1] \sin(\omega((i - 1) T - \tau_2)) \right] \]  

To calculate the power spectrum \( S_{\text{jitter}}(f) \) of the sampling noise we form the autocorrelation function

\[ r[i, p] = \text{Cov}(V_{\text{out}}^{\text{jitter}}[i + p], V_{\text{out}}^{\text{jitter}}[i]) \]  

To continue the analysis we need to make an assumption regarding the nature of the clock jitter \( \gamma_k[i] \). As previously stated, this depends on several factors and in this work we assume the clock source is a PLL dominatedly under the influence of white frequency noise in the VCO. Therefore, we may approximate the clock jitter with White Gaussian Noise having the following properties \( (k = \{1, 2\}) \)

\[ E(\gamma_k[i]) = 0 \quad \text{and} \quad \text{Var}(\gamma_k[i]) = \sigma^2 \]  

Hence we obtain

\[ r[i, p] \approx \begin{cases} \frac{A^2 \sigma^2}{\tau_1^2} \sum_{k=1}^{N} \sin^2(\omega(k T - \tau_2))/\tau_1^2, & p = 0 \\ -\frac{A^2 \sigma^2}{\tau_1^2} \sum_{k=0}^{N} \sin^2(\omega(i T - \tau_2))/\tau_1^2, & p = 1 \\ -\frac{A^2 \sigma^2}{\tau_1^2} \sum_{k=0}^{N} \sin^2(\omega((i - 1) T - \tau_2))/\tau_1^2, & p = -1 \end{cases} \]  

A time-average of \( r[i, p], \bar{r}[p] \), is made to get weak stationarity which, in turn, gives us \( S_{\text{jitter}}(f) \):

\[ S_{\text{jitter}}(f) = R(f) = \mathcal{F}_{\text{TD}} \{ \bar{r}[p] \} \]  

where \( \mathcal{F}_{\text{TD}} \{ \cdot \} \) is the time-discrete Fourier transform. We have

\[ \bar{r}[p] = r[i, p] \approx \begin{cases} \frac{A^2 \sigma^2}{\tau_1^2} (1 - \cos(2\pi f / f_s)), & \text{if} \ p = 0 \\ -\frac{A^2 \sigma^2}{2\tau_1^2}, & \text{if} \ p = \pm 1 \end{cases} \]  

and thus

\[ S_{\text{jitter}}(f) \approx \frac{A^2 \sigma^2}{\tau_1^2} \left(1 - \cos(2\pi f / f_s)\right) \]  

for \( f \in [-f_s/2, f_s/2] \). From the sampling noise power spectrum we may calculate the average inband sampling noise power

\[ P_{\text{noise inband}} \approx \frac{A^2 \sigma^2}{\tau_1^2} \left[ \pi \frac{\pi}{\text{OSR}} - \sin \left( \frac{\pi}{\text{OSR}} \right) \right] \]  

where OSR is the oversampling ratio \( f_s / f_T \). The ideal output signal (without sampling errors) can be approximated
Simulations of the $\Sigma\Delta$ sampler were made with MATLAB using the state equations of the circuit, assuming an ideal amplifier, and neglecting circuit noise. In reality, the amplifier sets an upper bound on the sampling frequency and input signal frequency. Moreover, noise coming from the resistor $R_1$, switches, and amplifier may, to some extent, decrease the benefit of using the proposed sampler. These issues will be investigated in future research. The difference between the simulations and the performance analysis is that the simulations take finite settling accuracy into account and also mismatch effects to a higher degree of accuracy. However, they both originate from the same differential equations.

All capacitors were set equal in size to ensure proper feedback operation. The switches were approximated with resistors, where an off-state is indicated by infinite resistance and an on-state is indicated by a finite resistance in the kΩ range. Accounting for varying on-resistance has little impact as long as the switches are wide enough to allow for full charge transfer. Of course, a “leaky” switch in the off-state will corrupt the operation of the proposed sampler but this has not been investigated here. Scaling the switches is also necessary to ensure that the voltage over the capacitors does not exceed the reference voltage $V_{\text{ref}}$.

The signal amplitude in the simulations was set to 0.1 V and $V_{\text{ref}} = 1$ V. Furthermore, for the above mentioned reasons we chose $R_1 = 3 \text{k}\Omega$, the switch resistances $R_{\text{sw}} = 0.4 \text{k}\Omega$, and the capacitors $C_i = 0.7 \text{pF}$ ($i = 1, 2, 3$). Throughout all simulations, the sampling frequency was $f_s = 96$ MHz, the signal bandwidth $f_B = 3$ MHz, OSR = 16, and sampling clock duty cycle $d_c = 0.25$.

### 4.1 Clock jitter $\sigma$ and signal frequency

The first simulation deals with inband SJNR versus signal frequency and is shown in figure 4. It is clear that the performance analysis and simulations have a strong correlation which means that the presented closed form expressions are useful for predicting performance. The SJNR of the $\Sigma\Delta$ sampler is roughly independent of the signal frequency, in contrast to the ordinary sampler. This is because of the factor $\sin^2(f_{\text{sig}}/f_s)$ in (19) which only drops by 4 dB as $f_{\text{sig}} : \{0 \rightarrow f_B\}$.

It is interesting to note that the SJNR of the $\Sigma\Delta$ sampler becomes higher than the SJNR of the ordinary sampler at a certain point in frequency given by

$$f_s \approx \frac{1}{\pi} \arcsin \left( \sqrt{\frac{1 - \sin(1/\text{OSR})}{2}} \right) \approx \frac{f_B}{\sqrt{3}} \approx 0.58f_B \quad (22)$$

where the approximation is quite accurate for OSR $\geq 10$. 

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**Figure 3.** SJNR comparisons of an ordinary sampler and the proposed $\Sigma\Delta$ sampler. On the left OSR = 1 and on the right OSR = 16. The clock jitter has a standard deviation of $\sigma = 10$ ps.
The next simulation is a sweep of clock jitter standard deviation ranging from \(0 \rightarrow 104\) ps using the same clock frequency of 96 MHz as before. The signal frequency is set to 2 MHz (66 % of the bandwidth). The result is shown in figure 5. The performance analysis and simulations, once again, have a strong correlation and the performance enhancement \(B_1(f_{\text{sig}})\) of using the \(\Sigma\Delta\) sampler, at this input signal frequency, is

\[
B_1(2 \text{ MHz}) = \frac{\text{SJNR}_{\Sigma\Delta}}{\text{SJNR}_{\text{ordinary}}} \approx \frac{\omega^2 \left( \frac{\sin^2(f_{\text{sig}}/f_s)}{2f_s^2} \right)}{1 - \sin\left(\frac{1}{\text{OSR}}\right)} \\
\approx 1.33 \approx 1.25 \text{ dB} \quad (23)
\]

Furthermore, the maximum performance improvement from using the \(\Sigma\Delta\) sampler rather than using an ordinary sampler is given by

\[
\max_{f_{\text{sig}} \leq f_B} B_1(f_{\text{sig}}) = \lim_{f_{\text{sig}} \rightarrow f_B} B_1(f_{\text{sig}}) \approx \frac{\pi^2 \sin^2(0.5/\text{OSR})}{2 \cdot \text{OSR}^2 \left(1 - \sin\left(\frac{1}{\text{OSR}}\right)\right)} \approx 4.75 \text{ dB} \quad (24)
\]

The last approximation is valid for \(\text{OSR} \geq 5\). Figure 6 shows a plot of the relation in (24) as function of the over-sampling ratio.

### 4.2 Matching

According to relation (6), the mismatch between \(C_1\) and \(C_2\) is dominant since usually \(\omega \tau_2 \ll 1\). The matching between the capacitors is important to ensure proper feedback operation. Figure 7a shows a sweep of the capacitor mismatch
standard deviation. The mismatch distribution is assumed to be Gaussian. It is clear that for common (∼0.1%) capacitor mismatches, there is no effect on the SJNR and distortion does not appear in the power spectrum for mismatches lower than (at least) 20% (see fig. 7b).

5 Conclusions

In this paper we have presented a new sampling circuit which shapes jitter induced sampling noise in the same way a ΣΔ ADC shapes quantization noise. We have made a thorough performance analysis of the proposed sampler and compared the results with an ordinary sampling circuit. To further strengthen the theoretical analysis, simulations with MATLAB were made using the state space equations of the ΣΔ sampler. The simulations and analytical results have shown a high level of agreement which makes the presented closed form expressions useful for predicting performance.

Mismatch effects have also been investigated to some extent. The mismatch between capacitors proves to be more important than switch resistance mismatches. Simulations show that the matching levels for capacitors of modern processes is more than sufficient to ensure distortion-free performance.

We have shown that the proposed sampler is suitable for wideband and bandpass applications where most of the signal power is high in the frequency band. Assuming a single tone at the upper bandwidth limit and an ideal amplifier, the ΣΔ sampler gives a 4.75 dB better jitter induced noise performance than the ordinary sampler.

References