Analysis of Timing Jitter in Inverters Induced by Power-Supply Noise

Adam Strak  
School of Information and  
Communication Technology  
KTH – Royal Institute of Technology  
Stockholm, Sweden  
Email: strak@kth.se

Hannu Tenhunen  
School of Information and  
Communication Technology  
KTH – Royal Institute of Technology  
Stockholm, Sweden  
Email: hannu@imit.kth.se

Abstract—This paper describes the transformation process of power-supply noise (PSN) to timing jitter of inverters. The focus is on the inverters used in multiphase clock-generator circuits (CGCs) commonly needed for Switched-Capacitor (SC) Sigma-Delta (ΣΔ) Analog-to-Digital Converters (ADCs). Closed form expressions relating timing jitter and PSN are presented and the results are compared with Monte-Carlo simulations performed in Spectre at BSIM3v3 transistor model level using the processes AMS 0.35µm and UMC 0.18µm. The PSN is assumed to have a white frequency distribution with independent power and ground noise. The results show that the transformation process is approximately linear and that the jitter impact decreases as transistors move deeper into the submicron domain. Furthermore, the transformation process is not symmetrical and is dependent on switching direction, even if the PMOS and NMOS sizings are such that the effects due to difference in hole and electron mobility are mitigated.

I. INTRODUCTION

The inverter is the fundamental building block in all digital electronics. However, inverters are not only used in digital electronics but sometimes also in analog blocks such as DLLs and VCOs. Furthermore they are also used in the intersection space between analog and digital, commonly referred to as mixed-mode or mixed-signal. One such application is depicted in fig. 1, multi-phase clock generation [1], often needed for Analog-to-Digital Converters.

Analog-to-Digital Converters are necessary building blocks in any mixed-signal system. As process feature sizes shrink and transistor speeds improve, ADC architectures traditionally used for low frequency applications, such as ΣΔ ADCs, become viable choices for use at higher frequencies. The principle behind the ΣΔ ADC is a trade-off between resolution in voltage and processing speed. Consequently, the analog parts of a ΣΔ ADC can usually be made simple and without the need of high matching accuracy. Furthermore, since the ΣΔ ADC has a larger content of digital blocks compared to most ADC architectures, it is well suited to be integrated with other digital circuits on the same chip.

Unfortunately, this means that the ADC becomes more vulnerable to PSN due to the limited isolation possibilities that come along with sharing the same die as noisy digital blocks. Naturally, analog blocks are very sensitive to PSN since they often depend on stable biasing for proper working conditions.

II. ANALYSIS MODELS

A. MOS Transistor Model

A modified version of the alpha-power (αP) law model [2] has been used in the mathematical analysis of the inverter. This model is summarized in eq. (1) for the NMOS (the PMOS has reverse voltage polarities and different physical parameters).

\[
I_{DSn} = \begin{cases} 
0 & \text{(off)} \\
K_{tn}(V_{GS} - V_{Tn})^{\alpha_n} & \text{(tri)} \\
K_{sn}(V_{GS} - V_{Tn})^{\alpha_n} & \text{(sat)} \\
-K_{rn}(V_{GD} - V_{Tn})^{\alpha_n} & \text{(rev)} 
\end{cases} 
\]  

However, also digital blocks are susceptible but the primary detrimental effect is not amplitude noise but timing noise or timing jitter. An ADC working with high signal frequencies will be strongly affected by timing jitter which means that any PSN that influences the CGC will add to tighten the jitter budget of the ADC.

This paper shows how PSN transforms into timing jitter in an inverter and gives closed form expressions that accurately predict the levels of timing jitter resulting from certain amounts of PSN. Previous work, such as e.g. [2], [3], [4], [5], and [6] have given approximations to the propagation delay of an inverter at low input frequencies with no regard for PSN. This work is part of a larger effort to characterize the different building blocks of CGCs to give a designer means of comparing which architecture is least sensitive to PSN from a jitter stand-point.
The process dependent parameters \( \{ K_{in}, K_{sn}, K_{rn} \} \) are given by

\[
K_{in} = \frac{I_{D0n}}{\left( V_{DD} - V_{Tn} \right)^{\alpha_n}/2} \\
K_{sn} = \frac{I_{D0n}}{\left( V_{DD} - V_{Tn} \right)^{\alpha_n}} \\
K_{rn} = \frac{I_{Drn}}{\left( V_{Drn}(V_{DD} - V_{Tn}) \right)^{\alpha_n}/2}
\]  
(2)

where \( I_{D0n} = I_{DS} \) at \( V_{GS} = V_{DS} = V_{DD} \), \( I_{Drn} = I_{SD} \) at \( V_{SG} = V_{DD} \) and \( V_{SD} = V_{Drn} \), \( I_{D0n} \) = \( V_{DS, sat} \) at \( V_{GS} = V_{DD} \), and \( V_{Drn} = V_{T, DB} \) is the threshold voltage of the drain-bulk diode. Furthermore, the different operating regions are

- (off): \( V_{GS} < V_{Tn} \) or \( V_{SG} < V_{Tn} \) if \( V_D < V_S \)
- (tri): \( V_{DS} < V_{D0n}^f \)
- (sat): \( V_{DS} \geq V_{D0n}^f \)
- (rev): \( V_D < V_S \)

where \( V_{D0n}^f = V_{D0n}((V_{GS} - V_{Tn})/(V_{DD} - V_{Tn}))^{\alpha_n}/2 \). The difference between this modified \( \alpha \) P law model and the model presented in [2] is the added reverse\(^1\) region since the forward triode region is insufficient in providing the desired accuracy in an overshoot/undershoot situation. The \( \alpha \) P law model was developed to provide a simple, yet realistic MOS model that has good accuracy for a full-range transient process such as the switching operation of an inverter. However, when working in reverse mode, only a limited range of the characteristic is traversed which introduces non-negligible errors in modelling a fast transient response.

\(^1\)By reverse we mean reverse triode since the DB diode will start conducting well before a reverse saturation region can be reached.

The differential equation describing \( dV_{\text{out}}(t)/dt \) during the switching process is given by eq. (5), where \( C_t = C_M + C_{DBn} + C_{DBp} + C_{L1} + C_{L2} \), \( I_n \) is the NMOS drain-source current, and \( I_p \) is the PMOS source-drain current.

\[
V_{\text{out}} = \frac{C_M}{C_t} \dot{V}_{\text{in}} + \frac{I_p - I_n}{C_t} + \frac{C_{L1} + C_{DBP}}{C_t} \delta V + \frac{C_L2 + C_{DBn}}{C_t} \delta G
\]  
(5)

Because the PSN originates from other logic blocks switching transients, an assumption about the frequency content of the PSN has been made such that the two last terms in (5) can be neglected. This is a reasonable assumption given the processes parameters used for this work (AMS 0.35 \( \mu \)m and UMC 0.18 \( \mu \)m), the normal propagation time of an inverter in either of these processes (~80 ps and ~30 ps) and the assumed steep input slope (\( \tau_{0.35} = 10 \) ps and \( \tau_{0.18} = 5 \) ps).

During a switching transient, the NMOS and PMOS transistors go through several operation regions. For an input low-high (HL) transient the transistors go through the following regions:

1) \( t \in [0, t_n] \): NMOS off, PMOS rev.
2) \( t \in [t_n, \min\{t_p, \tau\}] \): NMOS sat, PMOS rev.
3) \( t \in [\min\{t_p, \tau\}, \max\{t_p, \tau\}] \): NMOS sat, PMOS off/rev.
4) \( t \in [\max\{t_p, \tau\}, \min\{t_f, t_{\text{end}}\}] \): NMOS off, PMOS sat.
5) \( t \in [\min\{t_f, t_{\text{end}}\}, t_{\text{end}}] \): NMOS tri, PMOS off.

\( t_n \) denotes the time when the NMOS turns on, i.e. when \( V_{\text{in}}(t) - \delta G(t) = V_{Tn} \). Similarly, in a LH situation, \( t_p \) denotes the time when the PMOS turns off, i.e. when \( V_{\text{out}}(t) - V_{\text{in}}(t) < -V_{Tp} \). \( t_s \) denotes the time when the NMOS enters the triode region, i.e. when \( V_{\text{out}}(t) - \delta G(t) < V_{D0n}^f \). \( t_{\text{end}} \) denotes the time when \( V_{\text{out}}(t) \) crosses \( V_{DD}/2 \). During region 3, if \( t_p < \tau \), the PMOS is off which corresponds to a small and short overshoot scenario. The opposite represents a larger and longer overshoot.

It is clear that the region boundaries in a LH scenario are PSN dependent which means that an analytic treatment is not

\(^2\)For an input high-low (HL) transition, simply substitute NMOS with PMOS and \( n \) with \( p \).
possible. However, by making the approximations \( t_p \approx \tau \), \( t_1 \approx t_{\text{end}} \), and \( \{\delta_G(t), \delta_V(t)\} \approx \{\tilde{\delta}_G, \tilde{\delta}_V\} \) for \( t \in [0, \tau] \) we reduce the number of regions to three \((1, 2, \text{and } 4)\) and an analytical treatment becomes possible. \( \delta_G \) and \( \delta_V \) are defined as the time average, from 0 to \( \tau \), of \( \delta_G(t) \) and \( \delta_V(t) \) respectively. Because of the mentioned regions approximation (in both LH and HL scenarios), \( t_n \) will henceforth denote the time when the NMOS turns on during a LH transition and \( t_p \) will denote the time when the PMOS turns on during a HL transition.

\[
t_n = \left(\frac{V_{Tn} + \tilde{\delta}_G}{V_{DD}}\right) \tau, \quad t_p = -\left(\frac{V_{TP} + \tilde{\delta}_V}{V_{DD}}\right) \tau
\]  

B. Region 1: \( t \in [0, t_{(n,p)}] \)

During region 1 (LH) the NMOS transistor is off while the PMOS transistor works in reverse mode (due to the overshoot). The differential equation describing the output voltage is obtained by combining eqs. (5) and (1).

\[
V_{\text{out}} \approx c_{m1} \dot{V}_{\text{in}} - \frac{K_{\text{p}}}{C_{t1}} (V_{\text{out}} - V_{\text{in}} + V_{TP}) \frac{\alpha_p}{2} (V_{\text{out}} - V_{DD} - \tilde{\delta}_V)
\]

where \( c_{m1} = C_{M1}/C_{t1} \). This equation is analytically intractable. However, by noting that the second term is much smaller than the first due to the steepness of the input slope, we obtain

\[
V_{\text{out}}(t) \approx c_{m1} \dot{V}_{\text{in}} + V_{\text{out}}(0)
\]

This relation is valid both for a LH and HL transition, with \( V_{\text{out}}(0) = V_{DD} + \tilde{\delta}_V \) and \( V_{\text{out}}(0) = \tilde{\delta}_G \).

C. Region 2: \( t \in [t_{(n,p)}, \tau] \)

During region 2 (LH), the NMOS is saturated whereas the PMOS is still in reverse mode. By combining eqs. (5) and (1) and approximating the \( \alpha \)-power factors with constants, we obtain

\[
V_{\text{out}}(t) \approx (c_{m2} \dot{V}_{\text{in}} + V_{\text{out}}(0)k_{2i} - k_{2j})(t - t_j) + (c_{m1} \dot{V}_{\text{in}}t_j + V_{\text{out}}(0))(1 - k_{2j}(t - t_j))
\]

D. Region 3: \( t \in [\tau, t_{\text{end}}] \)

For the third region (LH), the NMOS is saturated while the PMOS is off. By, once again, combining eqs. (5) and (1) and approximating the ground bounce with its time average for \( t \in [\tau, t_{\text{end,ideal}}] \) we get

\[
V_{\text{out}}(t) \approx V_{\text{out}}(\tau) + k_3(t - \tau)
\]

where

\[
k_{3L} = -\frac{K_{sn}}{C_{t3}} (V_{DD} - \tilde{\delta}_G - V_{TN})^{\alpha_n}
\]

\[
k_{3H} = \frac{K_{sp}}{C_{t3}} (V_{DD} + \tilde{\delta}_V + V_{TP})^{\alpha_p}
\]

Fig. 4 shows the accuracy of the approximated switching characteristic compared with a Spectre BSIM3v3.1 simulation using AMS 0.35\( \mu \text{m} \) process parameters and also a numerical solution to eq. (5). It is clear that the mathematical result is very close to the BSIM3 level simulation.

IV. PROPAGATION DELAY

By solving the equation \( V_{\text{out}}(t_{\text{end}}) = V_{DD}/2 \) for \( t_{\text{end}} \), we obtain the propagation delay

\[
t_{pdL} = \frac{\tau}{2} + \frac{V_{\text{HL}} + \tilde{\delta}_V}{V_{DD} - V_{TN}} \left( 1 + \frac{\alpha_n \tilde{\delta}_G}{V_{DD} - V_{TN}} \right)
\]

\[
t_{pdH} = \frac{\tau}{2} + \frac{V_{\text{HH}} - \tilde{\delta}_G}{V_{DD} + V_{TP}} \left( 1 + \frac{\alpha_p \tilde{\delta}_V}{V_{DD} + V_{TP}} \right)
\]
where

\[ V_{\text{LH}} = V_{\text{DD}} \left( \frac{1}{2} + c_{m2} \right) - \frac{K_{\text{sn}}}{C_{\text{L2}}} (V_{\text{DD}} - V_{Tn})^{\alpha_n + 1} \]  

\[ V_{\text{HL}} = V_{\text{DD}} \left( \frac{1}{2} + c_{m2} \right) - \frac{K_{\text{sp}}}{C_{\text{L3}}} (V_{\text{DD}} + V_{TP})^{\alpha_p} \]

\[ \nu_{\text{LH}} = \frac{K_{\text{sn}}}{C_{\text{L2}}} (V_{\text{DD}} - V_{Tn})^{\alpha_n} \]  

\[ \nu_{\text{HL}} = \frac{K_{\text{sp}}}{C_{\text{L3}}} (V_{\text{DD}} + V_{TP})^{\alpha_p} \]  

(19)

(20)

(21)

Fig. 5 shows how the propagation delay varies with the ground potential, \( \Delta t_{\text{pd}} = t_{\text{pd}}(\delta_G, \delta_V) - t_{\text{pd}}(0, 0) \). As expected, the LH propagation delay increases with \( \delta_G \) since the NMOS is primarily conducting and \( \delta_G \) is directly affecting the NMOS \( V_{GS} \). Also, the HL propagation delay decreases with an increase in \( \delta_G \) since the PMOS is primarily conducting and \( \delta_G \) sets the initial \( V_{\text{out}} \) condition. The deviation between closed form expressions and Spectre at large \( |\delta_G| \) is mainly attributed to the larger size of the PMOS transistor which makes the LH overshoot larger than the HL undershoot. This, in turn, degrades the approximation that the PMOS turns off at \( t = \tau \) (LH transition). However, in general, the approximations still have good correspondence with BSIM3 level simulation results.

V. TIMING JITTER INDUCED BY POWER-SUPPLY NOISE

To calculate the timing variations due to PSN we take the variance of (17) and (18). By observing the previous assumption of white PSN with independent noise for ground and power we get

\[ \sigma_j^2_{\text{LH}} \approx \sigma_{\text{VDD}}^2 + \frac{V_{\text{LH}}^2 \alpha_n^2 \sigma_{\text{VDD}}^2}{\nu_{\text{LH}}} \]  

\[ \sigma_j^2_{\text{HL}} \approx \sigma_{\text{VDD}}^2 + \frac{V_{\text{LH}}^2 \alpha_p^2 \sigma_{\text{VDD}}^2}{\nu_{\text{HL}}} \]  

(22)

(23)

Fig. 6 shows a comparison of eqs. (22) and (23) and the jitter magnitude obtained with Monte-Carlo simulations in Spectre using BSIM3v3.1 and BSIM3v3.2 level transistor models with AMS 0.35 \( \mu \)m and UMC 0.18 \( \mu \)m process parameters. Note that the physical parameters used for plotting eqs. (22) and (23) were taken from the AMS 0.35 \( \mu \)m process whereas the simulation using UMC 0.18\( \mu \)m process parameters is intended as a reference showing the trend of the PSN impact when the feature size is scaled down.

The simulation was done using four \{ \( \delta_G, \delta_V \) \} samples per transition over 1000 LH and 1000 HL transitions. For each transition, the propagation delay was calculated and binned into a histogram (see fig. 7). The standard deviation of the histogram was used as an estimate of \( \sigma_j \).

VI. CONCLUSION

This work has presented a mathematical analysis of how PSN transforms into timing jitter in an inverter, a vital part in a multi-phase CGC. Simple, closed form expressions have been presented giving a designer a good idea of how circuit level considerations influence jitter performance based on the PSN environment. The closed form expressions that have been presented have a high level of agreement with BSIM3v3.1 level Monte-Carlo simulations using AMS 0.35 \( \mu \)m parameters.

REFERENCES


