Low noise and low cost neural amplifiers

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Abstract—Extracellular neural signal acquisition requires low noise, high gain, low power, and low cost amplifiers. This paper presents amplifiers with a simple architecture that ensures a good compromise among these characteristics. We present three amplifiers based on the same architecture, in which the first stage is a differential pair, respectively based on HBT, NMOS or PMOS transistors. The HBT-based solution presents the lowest intrinsic noise, followed by the NMOS solution. We use Monte Carlo simulation to validate the robustness of amplifiers’ characteristics of technological dispersions.

I. INTRODUCTION

Biomedical applications imply specific constraints on the design of electronic circuits. For integrated circuits, these constraints are not always in phase with the design rules in standard signal processing applications. We focus in this paper on emerging applications that necessitate the real-time acquisition of individual neurons’ electrical activity. We can mention among these applications the insulin control relying on beta-cells activity [1], the brain-machine interfaces [2], or the closed-loop systems for hybrid (living-artificial) neural networks [3-6].

All these applications use arrays of extracellular electrodes integrated on discrete probes or on chips. The advantages of this kind of interface, compared to the intracellular electrode solution, are make easier the multisite access and increase the living cells’ lifetime. But using extracellular electrodes also implies dealing with two issues: the low amplitude of acquired neural signal (10-100µV) and its high noise level (millivolts at low frequencies). A low noise, high gain, and filtering electronic amplifier is then necessary to process each signal. But, a low consumption and a small silicon area are also crucial constraints. With such an amplifier, a system will be able to process in parallel many neural channels, either when the density of electrodes is high or when their arrangement is complex. Fig. 1.a. presents the architecture such a system organized in a closed-loop where living neurons in vitro cultures communicate in real-time with an artificial unit, through an electronic interface. In Fig. 1.b., we identify the amplifying electronics on the acquisition channels.

This paper compares the characteristics of three “neural” amplifiers designed for processing neural signals. The amplifiers differ by their first stage based on a differential pair of: HBTs, NMOS transistors, PMOS transistors. Section II details the design of architecture and the resulting schematic chosen to optimize the performances. Section III shows the simulation results and performances of three configurations.

II. AMPLIFIER DESIGN

In neural amplifiers, the classical compromise in IC design between performances and cost becomes a key issue. Table I summarizes information on neural amplifiers described in the literature. Optimized component consumption and silicon area will limit the global cost (for fabrication and use). The technological process is also taken into account: choosing a BiCMOS process increases the fabrication cost. Performance features mentioned here are the equivalent input noise and the intrinsic gain; but the cutoff frequency, the slew rate, and the rejection of power supply noise are also important and will be specified in the presentation of our amplifiers.
### Table I. Some Neural Amplifiers

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Gain (dB)</th>
<th>Noisea (µVrms)</th>
<th>Consumption (W)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>36</td>
<td>9</td>
<td>98µ</td>
<td>0.35</td>
</tr>
<tr>
<td>[8]</td>
<td>38.9</td>
<td>9.2</td>
<td>68µ</td>
<td>0.177</td>
</tr>
<tr>
<td>[9]</td>
<td>39.3</td>
<td>7.8</td>
<td>115µ</td>
<td>0.107</td>
</tr>
<tr>
<td>[10]</td>
<td>40</td>
<td>15</td>
<td>330µ</td>
<td>0.076b</td>
</tr>
<tr>
<td>[11]</td>
<td>40</td>
<td>0.3</td>
<td>1.3m</td>
<td>0.3</td>
</tr>
<tr>
<td>[12]</td>
<td>40</td>
<td>2.2</td>
<td>80µ</td>
<td>0.16</td>
</tr>
<tr>
<td>[13]</td>
<td>51</td>
<td>3</td>
<td>775µ</td>
<td>0.52</td>
</tr>
<tr>
<td>[14]</td>
<td>60</td>
<td>3</td>
<td>1.7m</td>
<td>0.35</td>
</tr>
<tr>
<td>[15]</td>
<td>61</td>
<td>0.8</td>
<td>20m</td>
<td>Discrete</td>
</tr>
<tr>
<td>[16]</td>
<td>60 - 80</td>
<td>3.1</td>
<td>3m</td>
<td></td>
</tr>
<tr>
<td>[17]</td>
<td>70 - 94</td>
<td>1</td>
<td>130m</td>
<td>Discrete</td>
</tr>
</tbody>
</table>

a. Input equivalent noise, in the bandwidth between 100 Hz and 10 kHz.
b. Without the feedback circuit.
c. BiCMOS technology.

The neural amplifiers are intended to be part of a highly integrated closed-loop hybrid system [4], which simplified schematic is shown in Fig. 1. In such a system, extracellular electrodes are integrated on a Multi-Electrode Array (MEA) device [18], on which are placed cell cultures (dissociated cultures of rat embryonic cells). It processes in parallel 60 acquisition and stimulation channels. The amplifiers are optimized to be integrated as close as possible to the MEA, to limit external noise injection. We plan for a short term perspective to integrate the amplifiers directly on the MEA die. Their design considerations are:

#### A. Gain and intrinsic noise

These two factors are linked by the Friis formula, as expressed below:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_n - 1}{\prod G_i} \quad \Rightarrow \quad F = F_1$$  \hspace{1cm} (1)

Where $F_n$ and $G_n$ are the noise factor and the gain of $n^{th}$ stage.

A high first stage gain ($G_1$) reduces the influences of other stages. As observed in the literature, two solutions exist for setting the amplifier gain: in systems where the signal processing functions and the neural amplifier are embedded on the same die [7-13], $G_1$ is around 40 dB; in systems where the signal post-processing is separated from the amplification, $G_1$ is fixed around 60 dB or even higher [14-17]. We chose the second solution, which is less selective, in order to have the possibility to choose whether to integrate the post-processing functions together with the amplifiers or not.

Due to the biophysical specificities of neural activity, the information is contained in the range [100 Hz; 10 kHz]; experiments showed also that first order cut-off frequencies are efficient enough to discriminate this band width [7-17]. We implement a first order band-pass filter between 100 Hz and 10 kHz to eliminate the high level noise (some millivolts) existing at low frequencies and the environment noise at high frequencies. With this filter, the neuron activity (spike) can be discerned from noise, in an extracellular acquisition [19].

For our application, we fix the polarization of first and the second stages to, respectively, 10 µA and 5 µA. Each amplifier active area is limited to 1000 µm²; this constraint is imposed by the BiCMOS configuration die area.

#### B. Operating frequencies and slew rate

These two characteristics are secondary in our application. First, the signal’s bandwidth is quite low, as explained in II.A. Second, the amplifier load is the post-processing unit and is custom designed. It is so well-controlled and has high input impedance. At this point, the costs limitations are privileged, in two ways: (a) the classical third stage, with high current gain, is not implemented. This case is well explained in [20]; (b) the Miller capacitor is used both: for setting the high cut-off frequency (about 10 kHz) and for the classical phase compensation. The resulting phase margins for the three amplifiers are around 45 degrees.

#### C. Power supply noise

Another important noise source in an amplifier is the power supply noise. We test three alternatives for the first stage: (a) a cascoded first stage [21], (b) a passive equilibrated load for the first stage, and (c) a classical simple differential pair with active load. The additional area and consumption costs to achieve (a) and (b) are prohibitive. The classical architecture (c) provides a good compromise between performance and cost, and is finally chosen.

#### D. Neural amplifier schematic

The schematic resulting from the technical choices described in the previous paragraphs is shown in Fig. 2, in the HBT configuration. It includes two stages; the first stage is based on a simple differential amplifier of HBTs, NMOS or PMOS transistors with an active load; the second is a common source with an active load. The Miller phase compensation circuit provides the high cutoff frequency and a good stability.

![Figure 2. The HBT based amplifier’s architecture](image)

### III. RESULTS AND DISCUSSION

#### A. Amplifiers active part

The three configurations of amplifier are designed to fit the application’s constraints. The chosen technology is the 0.35µm HBT-BiCMOS technology from austria microsys-
tems™ and the design and simulation tools are from the Cadence™ suite. Table II summarizes the performances of HBT, NMOS and PMOS versions, simulated in open-loop. To estimate the effects of mismatch and process variations, we run Monte Carlo simulations.

A first statement from Table II is that the HBT-based amplifier presents the best noise figure. This result was expected, as the bipolar transistor is based on a volume current displacement, while the MOS transistors has a current displacement predominant in surface [22]. This good result is compensated by the high fabrication cost of a BiCMOS process compared to a CMOS process.

Analyzing the differences between two others solutions, the preconception that PMOS differential pairs are better in noise than NMOS ones falls down. This affirmation is based on the comparison between NMOS and PMOS transistors with an identical transconductance ($g_m$). Some well-known and efficient methods to design amplifiers (e.g. [20]) are based on the evaluation of $g_m$ necessary to reach predetermined performance (equivalent noise, slew rate …). For an equivalent $g_m$, a PMOS transistor occupies a largest silicon area than a NMOS transistor (for the selected process the electron and the hole mobility are, respectively, 370 and 126 cm²/V.s). As a larger area goes together with a smaller charge carry density, and as the noise level increases with the carry density, a PMOS-based amplifier presents a lower noise characteristic than the NMOS-based (for an equivalent $g_m$).

However, as our comparison rule is to keep constant the area and the consumption (see II.A), and not $g_m$, our conclusion is different. With the same biasing and area, the NMOS-based amplifier presents a higher $g_m$. As the carry density is lower in the NMOS-based amplifier, the noise figure is better.

Considering the power supply noise rejection, the three amplifiers present equivalent characteristics. The transfer function shows a maximal gain value under 0.4. In the signal bandwidth, it is reduced to 0.2 at worst (Fig. 3).

To summarize, the best noise and gain figures are obtained with the HBT-based amplifier. When considering also the fabrication cost, a NMOS-based amplifier implemented using a simple CMOS technology is also a solution. Finally, the power supply noise rejection is strongly linked to the architecture, and is not a discriminatory criterion.

### Table II. Performances of Three Versions of Neural Amplifier

<table>
<thead>
<tr>
<th>Config.</th>
<th>Gain (dB)</th>
<th>Noise (µVRMS)</th>
<th>Fc (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBT</td>
<td>110±1</td>
<td>1.65±0.05</td>
<td>15</td>
</tr>
<tr>
<td>NMOS</td>
<td>98±1</td>
<td>3.8±0.1</td>
<td>11</td>
</tr>
<tr>
<td>PMOS</td>
<td>95±1</td>
<td>4.5±0.1</td>
<td>10</td>
</tr>
</tbody>
</table>

*a. Gain and Noise are shown as (mean ± standard deviation), obtained from a 400-trial Monte Carlo simulation, considering mismatch and fabrication variations.

*b. Input equivalent noise, in the bandwidth [100Hz; 10 kHz].

### B. Amplifier with filter

We consider now the circuit including the filtering circuitry (Fig. 4). The feedback resistance $R_2$ sets the gain and, with the capacitor $C_c$, defines the high cutoff frequency. The frequency response curves are superimposed for the three configurations, and respect the specifications. We present in Fig. 5 and Table III simulation results from a Monte Carlo simulation with 400 trials, considering mismatch and process variations.

The low cutoff frequency is around 100 Hz. It is important to mention that this parameter depends on the output impedance of extracellular electrodes. More precise simulations should take in to account the electrode model, which is difficult to established, due to the high variability of experimental environment (electrodes and biological medium). However, if we consider standard models [23], the cutoff frequency stays in the 100Hz range.

Finally, the noise figures for the amplifiers with filter stay unchanged. The HBT-based amplifier is still the most performing solution, followed by the NMOS-based one.
TABLE III. GAIN VALUES AT 3 FREQUENCIES, FROM FIG. 4.

<table>
<thead>
<tr>
<th>Label</th>
<th>F (Hz)</th>
<th>Gain (dB)</th>
<th>Min.</th>
<th>Mean</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>100</td>
<td></td>
<td>54</td>
<td>55</td>
<td>56</td>
</tr>
<tr>
<td>B</td>
<td>1000</td>
<td></td>
<td>59</td>
<td>61</td>
<td>63</td>
</tr>
<tr>
<td>C</td>
<td>10 000</td>
<td></td>
<td>57</td>
<td>58</td>
<td>59</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

This paper compares three integrated amplifiers dedicated to the processing of neural electrical activity measured using extracellular electrodes. The three versions differ by their first stage, designed, respectively, with a HBT, a NMOS, and a PMOS differential pair. After defining the specifications, we discussed the amplifiers characteristics: intrinsic noise, gain, operating frequencies, slew rate, and rejection of power supply noise. We also discussed costs issues, characterized by power consumption and silicon area. From these considerations, we defined a common architecture for the three amplifiers. Simulations using Monte Carlo technique for the chosen process showed that all amplifiers present the requested frequency response. If we take into account the other characteristics, the HBT-based solution is optimal, except for the fabrication cost. If a CMOS technology is mandatory, the NMOS-based solution is the best one. Both HBT and CMOS versions will be implemented on prototype chips, and connected to a MEA device to measure the activity of cultured cortical cells. This circuitry will be included in a integrated closed-loop platform running hybrid neural networks [4]. The platform currently uses commercial neural amplifiers based on discrete components [6, 15]. The integrated solution will strongly increase the precision and the reliability on the cultured neurons' activity measurement.

REFERENCES