A 1-V, 10-bit Rail-to-Rail Successive Approximation Analog-to-Digital Converter in Standard 0.18µm CMOS Technology

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ABSTRACT

Two architectures for a 1-V, 10-bit 200-kS/s successive approximation analog-to-digital converter (ADC) implemented in a standard CMOS 0.18 µm digital process are presented. A track-and-hold circuit based on a novel implementation of the bootstrapped low-voltage analog CMOS switch with a novel rail-to-rail track-and-latch comparator circuit is described. A pMOS-only ladder containing a rail-to-rail current-to-voltage converter, performs the DAC function in the second ADC topology whereas a conventional R-2R ladder is used in the first one. Successive approximation and control logic is implemented using of a robust single clock phase D flip flop.

1. INTRODUCTION

Analog-to-digital conversion can be accomplished in numerous ways, but apart from flash converters, only successive approximation methods of analog-to-digital conversion (ADC) are well known for producing accurate, medium speed conversion of analog signals. It is a feedback scheme that uses a trial-and-error technique to approximate each analog sample with a corresponding digital word. It contains a track-and-hold stage as well as a digital-to-analog converter (DAC), a successive-approximation register (SAR) with control logic and finally a voltage comparator. The accuracy of conversion is mainly limited by the precision of component matching in the DAC and the ability of the comparator to accurately resolve small voltage differences between the analog input and the DAC output. The speed is directly related to the DAC settling time combined with the comparator settling time (to some desired accuracy). The overall speed of a successive approximation converter (SAC) is determined by the amount of time required for the execution of each comparison step.

In many mixed-signal systems, ADCs are required for interfacing analog signals to digital circuits. The requirement is usually to integrate these ADCs with digital signal processors (DSPs) in a low cost CMOS technology.

During the last few years much effort has been put into the reduction of the supply voltage and the supply power of mixed signal CMOS systems. This is primarily due to the increasing importance of battery-powered electronics, and the continued down-scaling of device sizes. Three main reasons can be given for the necessity of low-voltage circuits. The first one comes from the continued down-scaling of device feature size. As the channel length is scaled down to submicrons and the gate-oxide thickness becomes only several nanometers thick, the supply voltage has to be reduced (down to 1.5 V and below in the near future) [1] in order to ensure device reliability. The second reason is due to the increasing components on chip. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic function per unit area, the power per electronic function has to be lowered in order to prevent overheating of the chip. The third reason is dictated by portable, battery-powered equipment. In order to have an acceptable operation period from a battery, both the supply power and the supply voltage have to be reduced.

As a result, an ADC’s that are integrated with a DSP is required to operate in the same range of supply voltage. However, designing the ADC to operate at such a low supply voltage presents a great challenge, which comes from the fact that the threshold of MOSFET devices does not seem to be reduced at the same rate as the supply voltage. A particular consequence of the lowered power supply voltages is the need for rail-to-rail input stages in order to compensate for the reduced input common-mode and dynamic range. Therefore low-voltage analog circuit design becomes particularly difficult because the small available headroom severely limits the trade-offs among dynamic range, linearity, speed and power dissipation. To address this challenge, different techniques have been used to realize ADCs including the use of specialized processes that provide low-threshold devices [2], bootstrap techniques [3] and switched-opamp techniques [4]. In [5] a 1-V SAC using resistor based sample-and-hold circuit has been reported. This paper presents two different and novel design solutions for the very low-voltage rail-to-rail (1-V) successive approximation ADC in a standard CMOS process. The ADC was designed for low-power medium resolution applications such as data acquisition. The block diagram of the ADC is shown in Figure 1. The major analog and digital building blocks are discussed in section 2 and preliminary results are introduced in section 3.

2. LOW-VOLTAGE CONVERTER SYSTEM

2.1. Track-and-Hold Circuit

Most ADCs typically employ a sample-and-hold circuit at the front-end that must achieve high speed, high linearity and high precision with low-power dissipation. In low-voltage systems, analog sampling becomes particularly difficult because the available headroom severely limits the tradeoffs among dynamic range, linearity, speed and power dissipation.

The most serious factors affecting the performance of a high precision CMOS sample-and-hold circuit are charge injection and clock feedthrough. Several methods have been proposed to overcome these problems. These include the use of a dummy MOS transistor for charge cancellation, a compensation network for offset cancellation, a closed-loop architecture, a Miller hold capacitance and a switched-opamp based sample-and-hold circuit. Although charge cancellation methods that make use of a dummy transistor...

produce good simulation results, great care must be exercised when laying out the clock tree controlling the complementary switches. Others methods have either limited input bandwidth or introduce high design complexity. To overcome these limitations we propose a novel track-and-hold circuit based on the dummy compensated bootstrapped switch.

The track-and-hold scheme is depicted in Figure 2a while the control circuit (with pMOS-type pass devices) is shown in Figure 2b. Several issues have been considered in the type of transistor for the pass device (i.e., nMOS or pMOS). The most important from a dynamic linearity viewpoint are the ON-resistance RN and the channel charge Qch. All of these parameters scale with switch size; in the N-well process used where kp = 4×kp, kp = μCox, a pMOS device will consume 4 times the area of a nMOS device. However, a pMOS device exhibits a relatively constant conductance and channel charge, independent of the input signal, and can therefore be more easily compensated. Hence, we use a pMOS device as the pass device. The dummy analog bootstrapped switch is shown in Figure 2c and a detailed description of the circuit is given in [6].

2.2. Rail-to-Rail Comparator

To optimize the performance of a comparator, one has to consider the resolution, speed and power dissipation trade-off (in a situation of reasonable devices size, i.e. offset considerations). To achieve high resolution, large gain structures are necessary. Attempting to achieve this with one power-efficient gain stage results in reduced bandwidth due to amplifier gain-bandwidth trade-off. Conversely, medium-speed operation can be obtained by cascading several lower-gain stages at the expense of higher power dissipation. Although individual stages can be made fast, signals require time to propagate through all the stages. Possibly the most power-efficient high-speed design method involves combining a low-gain (high-bandwidth) stage with a positive feedback track-and-latch circuit. In essence, this achieves a large nonlinear gain with a high-speed and low power design as reported in [7]. Its main limitation is the required supply voltage. To overcome this, a novel rail-to-rail low-voltage comparator is proposed in Figure 3. The body of all the pMOS (nMOS) devices in the circuit is connected to the positive (ground) supply voltage VDDA (VSSA) unless otherwise stated.

The heart of this circuit is a regenerative latch. The regenerative output latch is based on an approach proposed in [8]. However, this circuit has a reduced input range. Transistors (M3, M3A, M3CA, M3B, M3CB) with (M4, M4A, M4CA, M4B, M4CB) have been added. Their main purpose is to enable the operation of the circuit when the input voltage is close to ground (VSSA). A set-reset latch (not shown in the figure) is connected to the comparator output nodes.

2.3. Successive Approximation Register and Control Logic

The SAR of a n-bit ADC contains a n-bit register that is cleared prior to the start of the conversion process. The register bits are set one at a time to a high state and produce an input to the n-bit DAC. The control circuit is essentially a ring-counter. The heart of the SAR and the control logic, in the proposed implementation of Figure 1, is a robust single phase clocking D flip-flop circuit [9]. A pMOS static latch in the flip-flop is depicted in Figure 4. True single phase static D flip flops can be constructed by cascading two latches with different clock polarity. The flip flop has no limitation on the input clock slope.

2.4. Digital-to-Analog Converter Circuit

A wide variety of DAC architectures exist, ranging from very simple to complex. Each, of course, has its own merits. Voltage division, current steering and even charge scaling can be used to map the digital value into an analog quantity. However, some of these architectures may not be suitable for low-voltage design. Due to the voltage limitation induced by the transmission gate and capacitance implementation, a charge scaling DAC cannot be used for very low-voltage applications. The use of fringing capacitors and low-voltage, low-stress bootstrapped switches [6] overcome those limitations.

Two DAC structures have been used in the proposed ADC and will be briefly described below.

The first one uses the voltage mode R-2R ladder of Figure 5. An opamp is not needed due to the fact that the output voltage goes directly to a high impedance node. This configuration presents an advantage compared to a current mode R-2R ladder requiring an output opamp, as the opamp adds noise to the system [11]. Performance of the first topology is limited by the matching requirements of the resistance. This can be relaxed by using a segmented method for the four most significant bits [12].

Figure 6 is a pMOS-only R-2R ladder DAC based on a linear current division principle [13]. The output voltage requirement dictates the choice of pMOS over nMOS. The resolution of this DAC can be very high without trimming [14] and scales with technology. However, it requires a low-voltage current-to-voltage converter. The class AB rail-to-rail input/output opamp of Figure 7 is used with a resistor in a negative feedback configuration to realize this function. It is a modification of the circuit proposed in [15] to satisfy the low-voltage requirement. nMOS switches driven by a clock signal booster [6] are used in the circuit to enable the operation at ultra low-voltage. These switches can also be implemented using a pMOS bootstrapped arrangement [6]. If space constraints are concerned, only the input switches (S3-S4, S9-S10) need to be implemented using the bootstrapped method.

3. Preliminary Results

The proposed implementation has been simulated with HSPICE using BSIMv3. A 0.18 μm digital CMOS technology has been used. Threshold voltages are approximately 0.52 V and −0.48 V for nMOS and pMOS transistors respectively. A detailed performance analysis of the track-and-hold circuit has been reported in [6]. As a brief reminder, a resolution up to 16-bits is reachable with a load condition of 5 pF. The comparator was tested using the critical waveform reported in [7]. This waveform can be generated using an arbitrary waveform generator or by using the method reported in [16]. The simulated comparator performance using VDDA = 1.0 V, a switching voltage overdrive of ±0.1220 mV (which corresponds to ±0.5 LSB of a 12 bit precision), a 16.67 MHz clock signal and an inverter as a load is shown in Figure 8. The input was set to VDDA followed by 0.125×VDDA and has been simulated with a 2.22 MHz clock signal. The results are in Figure 9. Layout of key components (track-and-latch, comparator and DAC) has been submitted for fabrication some experimental results will follow soon.
4. CONCLUSION

In this paper, two design solutions to a rail-to-rail successive approximation DAC have been presented. The proposed methods can be used for the design of low-voltage high-speed and high-resolution pipelined ADCs. Layout of key components (track-and-latch, comparator and DAC) has been submitted for fabrication and some experimental results will follow soon.

REFERENCES


Figure 4: Low-voltage Latch circuit used in SAR

Figure 5: Low-voltage R-2R DAC

Figure 6: MOSFET-Only Current DAC

Figure 7: Low-voltage opamp used for current-to-voltage conversion

Figure 8: Comparator Simulation

Figure 9: Simulation of two conversions cycle