A CMOS DIGITALLY PROGRAMMABLE CURRENT STEERING SEMIDIGITAL FIR RECONSTRUCTION FILTER

Arshan Aga and Gordon W. Roberts

Microelectronics and Computer Systems Laboratory, McGill University
3480 University St., Montreal, Quebec, Canada H3A 2A7
{arsh roberts}@mcs.ece.mcgill.ca

ABSTRACT

A low power, area efficient, single bit finite-impulse response (FIR) reconstruction filter for delta-sigma applications based on a current steering approach is presented. The FIR filter coefficients are programmable with discrete values from -8 to +8, thus allowing for various filter responses including lowpass and bandpass transfer functions on the same chip. The filter is implemented in a 0.25 μm standard CMOS process and incorporates 2.09 mm² of active area and a 2.5 V supply. Three different filter functions are implemented: a voice band lowpass filter, an audio band lowpass filter and a bandpass filter. The audio band example achieves a dynamic range of 78 dB for a signal bandwidth of 20 kHz and 65 dB over a 100 kHz bandwidth.

1. INTRODUCTION

With the scalability and ease of testability of digital circuits, more and more emphasis is being placed on robust digital solutions to analog problems. A direct repercussion of this is the abandonment of traditional analog signal processing techniques and the emergence of DSP as the dominant method of signal processing. The bottleneck of such a methodology is the performance and speed limitations of the converters that are used to interface with the real world. The delta-sigma technique of conversion involves using oversampling techniques to trade off speed for performance.

An oversampled delta-sigma D/A converter using a traditional analog implementation for the reconstruction filter is shown in Figure 1(a). This architecture most commonly involves using a switched capacitor IIR or an active-RC implementation of the reconstruction filter. Both of these types of filters involve complex stability issues, relatively high power consumption, performance limiting operational amplifiers and area intensive passive components that do not scale well with technology.

A more elegant solution involves using an FIR semidigital reconstruction filter approach shown in Figure 1(b). This methodology not only is inherently stable but certain topologies can actually maximize the use of digital components thus making it scalable and increasingly area-efficient in sub-micron technologies.

Various topologies of the semi-digital reconstruction filter exist including: switched capacitor [1,2], current mode [3], switched current [4], and more recently current steering [5]. The major advantages of using the current steering topology compared to the alternative methodologies is that the relative analog proportion of the circuit is minimized and the static power consumption of the circuit is also minimized.

This paper involves the implementation of a 64-tap programmable version of an FIR current steering reconstruction filter in a 0.25 μm standard CMOS technology. The novel current steering structure used to realize the filter is a derivative of the structure given in [5]. The proposed structure allows for further maximization of robust digital components and extends the previous design to include coefficient programmability. Furthermore, a simpler and more power efficient output stage has been incorporated in place of the standard operational amplifier output stage. For audio band applications the filter achieves 78 dB of dynamic range for a signal bandwidth of 20 kHz and 65 dB over a 100 kHz bandwidth.

Basic concepts of the current steering FIR semidigital filter will be covered in section 2. Section 3 will focus on the implementation of the filter including the architecture and design methodology of various building blocks. Section 4 will present some experimental results obtained for a voice band lowpass example, an audio band lowpass example and a bandpass example. Also, the significance of the proposed structure will be verified by comparing the results with other documented topologies.

2. RECONSTRUCTION FILTER

2.1 Semidigital FIR Reconstruction Filter

The general architecture of the single bit semidigital N-th order FIR reconstruction filter is shown in Figure 2 and has a transfer function of the form:

\[ H(z) = a_1 z^{-1} + a_2 z^{-2} + \ldots + a_{N-1} z^{-N+1} + a_N z^{-N} \] (1)

where \( x[n] \) is the single bit digital input, \( y[n] \) is a discrete-time analog output and the coefficients \( a_j \) through \( a_N \) are analog in nature.

In order to take advantage of parallelism the summing operation is usually done in the current domain or the charge domain rather than
in a serial fashion (i.e., voltage). Furthermore, the coefficients of the FIR filter ideally can take on any value, but due to process limitations and matching issues, they are usually quantized.

2.2 Current Steering Topology

The difference between the various topologies of semidigital FIR filters is how the coefficients are formed. Current mode filters use individual weighted currents to form the coefficients while switched capacitor implementations use a ratio of capacitors. The current steering topology forms the coefficient \( a_i \) (the \( i \)-th coefficient) by steering a current proportional to this value from one branch to another using \( T_i \) differential pairs. A diagram of the novel current steering structure utilized in the proposed filter is shown in Figure 3. Here, digital signals \( Q_j \) and \( \overline{Q}_j \) correspond to the \( D \)-flip flop's positive and negative outputs, respectively. When the output is taken differentially, the \( i \)-th tap coefficient for this structure is given by:

\[
a_i = \frac{I_{i,\text{bias}}}{\sum_{k=1}^{N} T_k} \times 2 \times I_{\text{bias}}
\]  

(2)

This topology is based on the one used in [5] but with the use of a single cascaded current source in place of a single current source transistor with multiple cascaded transistors and differential pair switch banks at each tap instead of a single differential pair. These modifications allow for the maximization of digital components by removing the redundancy in the cascaded transistors which are large and analog in nature and replacing them with differential pair switch banks which are minimum sized and digital in nature. Furthermore, the onus of defining the \( i \)-th tap coefficients is shifted from the \( i \)-th cascode transistor to the \( i \)-th differential switch bank. As will be shown in section 3, defining the coefficient in this manner allows for programmability to be achieved through modifications in the digital switch bank transistors instead of the analog cascode transistor.

3. IMPLEMENTATION ISSUES

3.1 Current Source

The current source used is a PMOS cascaded current mirror with self-biasing [6] and an off chip resistor to generate the current as shown in Figure 4. The cascode mirror was used to boost the output resistance of the current source and minimize the effects of voltage glitches at the output node \( V_{\text{CUR}} \). The self-biasing scheme [6] allows for a simple, compact method of implementing the cascode current mirror with only a single biasing resistor. Finally, PMOS transistors were used in the implementation because their NMOS counterpart is susceptible to process variation in the body effect that could adversely alter the circuit performance.

3.2 Differential Pairs

The differential pairs that implement the coefficients were done using a cascaded architecture [7]. Figure 5 depicts the \( j \)-th programmable differential pair in the \( i \)-th stage of the scan chain. Digital signals, \( Q_j \) and \( \overline{Q}_j \), correspond to the positive and negative output of the \( i \)-th \( D \)-flip flop and are used to direct the current either to the \( I_{\text{out+}} \) or \( I_{\text{out-}} \) terminals. Also, \( I_{\text{bias}} \) can be set high/low in order to disable/enable the differen-
4. EXPERIMENTAL RESULTS

A 64-tap current steering semidigital FIR filter with programmable integer coefficients spanning from -8 to +8 was fabricated in a 0.25 µm CMOS process. The filter occupies a total active area of 2.09 mm² and requires a single supply of 2.5 V. A micrograph of the chip is shown in Figure 7.

Of the total active area only 0.09 mm² (4.3%) is occupied by analog circuitry consisting exclusively of current mirrors, while the rest of the area consists of robust and technology scalable digital circuitry. Furthermore, 45% of the active area is consumed by an area intensive scan chain used for shifting in the programming bits of each coefficient. For specific applications this area can be greatly reduced by narrowing the degree of programmability.

Three different filter responses were programmed into the FIR filter: a voice band lowpass filter, an audio band lowpass filter and a bandpass filter. The frequency responses of the three filters were found by stimulating the filter with a repeating impulse input at a clock rate of 1.5 MHz and observing the output with a spectrum analyzer. The measured frequency responses of the three filters (solid lines) are shown in Figure 8 together with their theoretical responses (dashed lines). Here, the theoretical responses correspond to the frequency responses of the filter when the ideal quantized coefficients are used.

As is evident from the plots in Figure 8, the measured frequency responses closely match the theoretical responses. A detailed analysis reveals that the cut-off frequencies deviate by no more than 2% in each case and a deviation of less than 0.3 dB exists in each of the passband regions. Visible deviations from the theoretical responses exist in the stopband regions which is attributed to process variation on the switches moving the zero positions from their theoretical locations. The net effect of these deviations is negligible since the minimum stopband attenuation is maintained to within 2 dB of the theoretical value in each case.

The dynamic performance of the filter for the audio band filter case is summarized in Figure 9. The filter achieves a peak signal-to-noise-plus-distortion ratio (SNDR) of 60 dB and a dynamic range of...
78 dB over a 20 kHz bandwidth and a peak SNDR of 52 dB and a dynamic range of 65 dB over a 100 kHz bandwidth.

A summary of the specifications obtained from the FIR filters implemented in [3], [4] and the current steering FIR filter proposed in this paper is shown in Table 1. Taking into account the process, tap length and degree of programmability it can be seen that the current mode and current steering topologies are quite comparable to one another in terms of area efficiency and both surpass that achieved by the switched current topology. Also, the power efficiency of the current steering topology over the other topologies is apparent. However, the dynamic range specification of this topology is inferior to that of the current mode filter. This lag in performance is most probably caused by the compounded glitching created by the switch banks during transitions in the circuit being insufficiently suppressed by the use of the cascaded switches, therefore giving rise to added noise and distortion in the system. Efforts to correct this problem are underway.

5. CONCLUSION

A semidigital programmable FIR filter using the current steering approach was implemented in a 0.25 μm standard CMOS technology. It was seen that this filter topology has the ability to achieve various filter functions simply by shifting in different control bits to switches. Furthermore, the area occupied by robust digital circuitry is maximized thus allowing for the design to be increasingly scalable with reduced feature sizes. A comparison between the various semidigital FIR filter topologies showed the power savings achieved by the filter but some improvements in the dynamic performance of the filter are required in order to achieve the dynamic range specification achievable by the current mode topology.

6. REFERENCES