A ROBUST DC CURRENT GENERATION AND MEASUREMENT TECHNIQUE FOR DEEP SUBMICRON CIRCUITS

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ABSTRACT

A robust and highly scalable technique for generating and measuring DC currents is described. The circuits consist largely of digital electronics except for two simple passive filters and a comparator. This simple structure is able to force a current into a node and measure the corresponding node voltage, and vice versa. The technique has been successfully demonstrated using a prototype constructed using an FPGA chip.

1. INTRODUCTION

Recent years have seen a rapidly increasing demand for highly integrated mixed-signal ICs. This is mostly driven by the ever-expanding communications industry. However, as the level of integration increases, more and more mixed-signal components are being buried deep inside large amounts of digital circuitry without any external I/O access. This creates a difficult problem for initial device and circuit characterization and diagnosis, as well as during a production test. For example, to measure the bias current for a high precision ADC circuit requires some form of external access. However, the access mechanism, such as a test bus, can introduce additional noise from off-chip sources.

In this paper, we are concerned with a method for on-chip current measurement and current sourcing, which we believe will be useful for characterizing a wide variety of circuits such as A/D converters, PLLs and bias networks. The traditional method for a forced-voltage current measurement is by using either a virtual ground amplifier [1] [2] or an integrating network [3]. However, all of these circuits involve the use of op-amps, which makes them relatively non-scalable for on-chip implementation. Traditional on-chip current sources reported in [4], [5] and [6] suffers from low output resistance and shifts in current levels due to process variation. These problems have rendered these circuits unsuitable for characterizing or diagnosing analog circuits, when accuracy and precision is emphasized.

In this paper, we used a simple ADC and a programmable voltage source to capture the DC transfer characteristic of a CMOS inverter at different current levels. Once known, the inverter transfer characteristic can be used indirectly to determine the value of an unknown current level with approximate 7-bits of resolution. A current sourcing mechanism can also be achieved in much the same way using the knowledge of the inverter transfer characteristic.

The rest of the paper is organized as follows: Section 2 presents the principle of current measurement using a CMOS inverter structure. Section 3 describes the method of generating a known current using the same inverter structure. In section 4, we discuss a prototype constructed using an FPGA and its experimental results. Finally, conclusions are provided in section 5.

2. CURRENT MEASUREMENT

2.1 Basic Principle

For the CMOS inverter shown in Fig. 1(a), its output, denoted \( V_{\text{out}} \), changes when either its input \( V_{\text{in}} \) or load current \( I_{\text{out}} \) changes as depicted in Fig. 1(b). We can express this functional relationship as:

\[ V_{\text{out}} = f(V_{\text{in}}, I_{\text{out}}) \quad (2.1) \]

Rearranging (2.1) so that \( I_{\text{out}} \) is expressed in terms of \( V_{\text{in}} \) and \( V_{\text{out}} \), we can write

\[ I_{\text{out}} = g(V_{\text{in}}, V_{\text{out}}) \quad (2.2) \]

which specifies the load current in terms of the input and output voltages of the inverter. The principle of the force-voltage measure current technique is to set \( V_{\text{out}} \) to a constant value \( V_{\text{ref}} \) through a feedback circuit by adjusting the value of the input voltage \( V_{\text{in}} \) using the circuit shown in Fig. 2(a). On doing so, the output current becomes a one variable function of \( V_{\text{in}} \) expressed as

\[ I_{\text{out}} = g(V_{\text{in}}) \quad (2.3) \]

Fig. 1 (a) CMOS Inverter, (b) Transfer function \( f(V_{\text{in}}, I_{\text{out}}) \)
A plot of \( g(V_{in}) \) for different values of \( V_{force} \) is shown in Fig. 2(b) for a typical CMOS inverter. If the functional relationship in (2.3) is known, one can force a voltage at the inverter output node \( V_{out} \) and measure the corresponding voltage at the inverter input node \( V_{in} \) and, subsequently, deduce the corresponding output current \( I_{out} \) using (2.3).

To obtain the functional relationship \( g(x) \), we first measure its inverse relationship, \( g^{-1}(x) \), by setting \( V_{force} \) to the voltage we want to force, and sweep the inverter load current \( I_{out} \) over a range of currents, followed by measuring the voltage at the input to the inverter, i.e., see Fig. 3. Once the inverse mapping is known, we can interchange the input and output variables to obtain \( g(x) \).

### 2.2 Current Measurement Circuit

The feedback network in Fig. 2(a) can be replaced by the digital sampling circuit shown in Fig. 4. When this system is in equilibrium, \( V_{out} \) equals \( V_{force} \). More importantly, the value of \( V_{in} \) is determined by the filtered value of the PDM bit-stream coming out from the D-type flip-flop (D-FF). By counting the number of 1’s at the D-FF output in a frame of \( 2^n \) bits, one can obtain an \( n \)-bit representation of \( V_{in} \) over the full scale range of \( V_{DD} \) to \( V_{SS} \).

The forcing voltage is generated by a programmable voltage reference described in [7], which consists of a PDM bit-stream generator (derived from a software implementation of a digital \( \Sigma \Delta \) modulator) and a first order RC low-pass filter (Fig. 5).

### 3. CURRENT GENERATION

#### 3.1 Basic Principle

If the \( I_{out} \) of the CMOS inverter shown in Fig. 2(a) is fixed to an arbitrary value \( I_{force} \), \( V_{out} \) can be expressed as a one-variable function of \( V_{in} \):

\[
V_{out} = f(V_{in})
\]  

(3.1)

Now if the inverter is connected to an unknown impedance and the output current is equal to \( I_{force} \), the values of \( V_{in} \) and \( V_{out} \) must follow the relationship in (3.1). Thus, given the inverse function \( f^{-1}(x) \), one can find the \( V_{in} \) required to satisfy (3.1) from the following expression:

<table>
<thead>
<tr>
<th>Entry #</th>
<th>Equivalent ( I_{ref} )</th>
<th>Measured ( V_{in} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-1.0000mA</td>
<td>0000 0001</td>
</tr>
<tr>
<td>1</td>
<td>-0.9375mA</td>
<td>0000 0101</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>16</td>
<td>0.0000mA</td>
<td>0110 1001</td>
</tr>
<tr>
<td>17</td>
<td>0.0625mA</td>
<td>0110 1100</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>30</td>
<td>0.8750mA</td>
<td>1111 1001</td>
</tr>
<tr>
<td>31</td>
<td>0.9375mA</td>
<td>1111 1110</td>
</tr>
</tbody>
</table>

Table 1 A 5-bit look-up table for the ammeter
The relationship in (3.2) exists if and only if $I_{\text{out}} = I_{\text{in}}$. A current source can be derived using building blocks to substitute the functions $f(x)$ and $f'(x)$. The configuration is shown in Fig. 6. It consists of an inverter and a lookup table. When this system is in equilibrium, the output current of the inverter is forced to $I_{\text{in}}$ for any arbitrary output voltage.

3.2 Current Sourcing Circuit

The feedback system in Fig. 6 can be implemented digitally using the structure shown in Fig. 7. The analog function $f'(x)$ in Fig. 6 is replaced by a voltmeter (A/D), a lookup table (RAM) and a programmable voltage source (D/A).

The programmable voltage source is the same as the one in Fig. 5. The voltmeter is implemented by a delta-modulator circuit found in [8] and [9], with the addition of a frame counter, as shown in Fig. 8. Similar to the feedback loop in Fig. 4, the voltage at both terminals of the comparator are equal when the system is in equilibrium. The frame counter calculates the density of 1’s from the PDM stream from the D-FF and thus the voltage $V_{\text{in}}$.

The lookup table needs to be calibrated whenever a new value of $I_{\text{in}}$ is required. It is calibrated using the exact same setup shown in Fig. 4. However, this time $I_{\text{out}}$ is fixed to the value of $I_{\text{in}}$ while the $V_{\text{out}}$ of the inverter is swept by varying $V_{\text{in}}$. The resultant lookup table lists the value of $V_{\text{in}}$ as a function of $V_{\text{out}}$. An example lookup-table is shown in Table 2.

After calibration, an unknown impedance can be applied to the output of the inverter. The control logic performs a binary search for the correct $V_{\text{in}}$ that satisfies (3.2), and hence forces a current of value $I_{\text{in}}$ into the load.

Using (2.2), we can compute the error of the sourced current according to the following

$$\frac{\Delta I_{\text{out}}}{I_{\text{out}}} = \frac{\Delta V_{\text{in}}}{V_{\text{in}}} + \frac{1}{r_o} \frac{\Delta V_{\text{out}}}{V_{\text{out}}}$$

(3.3)

where $\Delta V_{\text{in}}$ and $\Delta V_{\text{out}}$ are the errors associated to the finite resolution of $V_{\text{in}}$ and $V_{\text{out}}$.

The values $g_{\text{en}}$ and $r_o$ are parameters from the Norton equivalent circuit of the inverter illustrated in Fig. 9. If we denote the corresponding parameters of the PMOS and the NMOS transistor by $g_{\text{enPMOS}}$, $g_{\text{enNMOS}}$, $r_{\text{PMOS}}$ and $r_{\text{NMOS}}$ respectively, we can write

$$g_{\text{en}} = g_{\text{enPMOS}} - g_{\text{enNMOS}}, \quad r_o = r_{\text{PMOS}} + r_{\text{NMOS}}$$

(3.4)

Since $r_{\text{PMOS}}$ and $r_{\text{NMOS}}$ are constant at a particular bias current level, the only way to decrease the ratio $\Delta I_{\text{out}}/I_{\text{out}}$ is to decrease $g_{\text{en}}$. This can be done by using a smaller W/L geometry for the inverter.

4. EXPERIMENTAL RESULTS

A prototype of the two circuits was built and tested. The PDM Bit-stream Generator, the Frame Counter and the D-FF (in Figs. 4 and 8) were built with an Altera EPM7128S FPGA chip. The lookup table and the control logic were implemented in software using a Teradyne A567 mixed-signal tester. This choice was made to simplify the design process, since this prototype was intended for a quick proof of concept only. All other components were constructed with discrete components, including the core CMOS inverter (Motorola MC14007UB). The supply voltage was 5 V for all components except the voltage comparator, which ran on a ± 6 V supply. The system was clocked at 6.29 MHz.

<table>
<thead>
<tr>
<th>$V_{\text{out}} (8\text{-bits})$</th>
<th>Actual $V_{\text{out}}$</th>
<th>Measured $V_{\text{in}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000</td>
<td>0.00V</td>
<td>1111 1110</td>
</tr>
<tr>
<td>0000 0001</td>
<td>0.02V</td>
<td>1111 1101</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>1111 1110</td>
<td>4.96V</td>
<td>0000 0001</td>
</tr>
<tr>
<td>1111 1111</td>
<td>4.98V</td>
<td>0000 0001</td>
</tr>
</tbody>
</table>

Table 2 An 8-bit look-up table for the current source
The first experiments were to verify the linearity of the voltage reference source and the voltmeter. The components indicated good linearity for the intended 8-bit resolution. The DNL (INL) of the voltage reference was 0.023 (0.222) LSB, while a DNL (INL) of 0.180 (0.229) LSB was achieved for the voltmeter.

The next experiment was to demonstrate the system’s ability to force a voltage and measure a current. The system was calibrated to force the output node to 2.5 V while measuring a full scale current of ±6 mA with 7-bits of resolution. The maximum DNL (INL) was below 0.375 (0.255) LSB. Fig. 10 shows the ADC transfer function for a full-scale current of ±6 mA with 5-bits of resolution (32 levels). As can be seen from the figure, the linearity of the ammeter is clearly demonstrated.

The last experiment was to demonstrate the system’s ability to generate DC current signals. The transistors for the core CMOS inverter in this experiment were lengthened three times (using a series connection) to reduce the output current’s sensitivity towards quantization errors. The current source was calibrated for 8 different current levels from −2 mA to 1.5 mA with 0.5 mA increments. The results are shown in Fig. 11. The plot clearly indicates a current source with high output resistance. The current fluctuations for each current level are caused by the finite resolution of the on-board ADC and programmable voltage source. The maximum error for all positive currents was 0.018 mA for an output voltage range of 1.5 V to 4.5 V, while the error was 0.022 mA for all negative currents over an output voltage range of 0.5 V to 2.5 V. A minimum current error of 1.1% was achieved for the −2 mA source. The current accuracy is expected to improve for on-chip implementation of the inverter, where it will be easy to reduce the (W/L) ratio.

![Fig. 11 Sourced current for 8 different current levels](image)

**5. CONCLUSION**

A robust and simple current generation and measurement technique has been presented. It makes use of digital calibration using a combination of ADC and DAC that consists of several first-order passive filters, a comparator and a CMOS inverter. Experiments reveal that these circuits could measure currents with 7-bits of resolution, as well as generate currents with a minimum error of 1.1%. However, the most important aspect of this technique remains that most of the design is digital, enabling it to take best advantage of future technology scaling.

**6. ACKNOWLEDGMENTS**

This work was supported by the Natural Sciences and Engineering Research Council of Canada and Micronet, a Canadian network of centers of excellence dealing with microelectronic devices, circuits, and systems.

**7. REFERENCES**