Capacitance characterization of tapered through-silicon-via considering MOS effect

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In this paper, closed-form expression for the parasitic capacitance of tapered TSV (T-TSV) considering metal–oxide–semiconductor (MOS) effect is proposed by solving two-dimensional (2D) Poisson’s equation. ANSYS Q3D Extractor is employed to verify the proposed model for the slope wall angle of 75°, 80°, 85° and 90°. It is shown that error is less than 5%. The capacitance characterization of copper T-TSV is studied in detail, by taking slope wall angle of 80° for instance. The results show that the capacitance of T-TSV acts as that of MOS device in changing the bias voltage; the increases of the bottom radius of T-TSV (from 1 to 5 μm), dielectric liner thickness (from 0.1 to 0.5 μm), liner dielectric constant (from 1 to 5), T-TSV height (from 10 to 50 μm) and acceptor concentration (from $1 \times 10^{15}$ to $5 \times 10^{17}$ cm$^{-3}$) cause increase of T-TSV capacitance by about 25 fF, −12 fF, 12 fF, 210 fF and 12 fF, respectively. Finally, the condition for T-TSV simplified to cylindrical TSV is obtained.

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1. Introduction

With the continuous development of the semiconductor technologies node, the conventional planar integrated circuit (IC) scaling has reached limits that are difficult to surpass [1], processing complexity, and increasing fabrication cost. The chip scaling and functionality increase result in interconnect delay increase, limiting IC performance and increasing power consumption. To overcome these limitations, Moore’s law is replaced by the “more than Moore” vision [2,3]. Three-dimensional (3D) ICs offer the most promising platform to implement “more than Moore” technologies, bringing multiple design disciplines (Digital, analog, RF) and disparate process technologies (SOI, SiGe, GaAs, etc.) on a single chip by stacking semiconductor layers on top of each other [4], and sustain continuous increase in functionality, performance and integration density indefinitely [5]. Through-silicon-via (TSV) is the core technology that provides a vertical interconnection with greatly reduced interconnection length among the stacked dies [6–9]. Much work is needed to properly characterize and model these TSVs due to the introduced electrical parasitic. Accurate closed-form models of TSV provide an efficient method to characterize the performance of signal paths containing TSVs.

There are four main types of TSV profiles existing in the industry, namely, tapered, cylindrical, annular, and coaxial TSVs, respectively, depending on the etching processes applied to form TSVs. The tapered-TSV (T-TSV) has smaller reflection noise and signal loss, and eases the manufacturing process as well [10].

To the best of our knowledge, there are several papers [11–17] published on the analytical modeling of the resistance, inductance, and capacitance of cylindrical TSVs, and some studied on the coaxial [18–20] and annular [18,21] ones, while few focus on T-TSVs. It is noted that the closed-form expressions are proposed to calculate the parasitic resistance and inductance of T-TSV in [22]. However, TSV capacitance has the most predominant impact on circuit operation based on current TSV dimensions [10]. Accurate expressions for the capacitance of T-TSV have never been reported. Moreover, the study on T-TSV is more universal because T-TSV degenerates to cylindrical one as the slope wall angle is 90°. In this paper, closed-form expression for the parasitic capacitance of T-TSV is proposed by solving 2D Poisson’s equation based on the capacitance models of the dielectric liner and depletion region. The rest of this paper is organized as follows. In Section 2, MOS effect is introduced and closed-form expression for the capacitance of T-TSV considering MOS effect is presented. In Section 3, the proposed expression is verified by employing the electromagnetic field solver ANSYS Q3D Extractor [23], and the capacitance characterization of T-TSV is discussed. In Section 4, the condition for T-TSV simplified to cylindrical TSV is obtained. Finally, Section 5 concludes this paper.

The analysis in this paper is carried out for p-Si, but a similar analysis is applicable for n-Si substrate.

2. Closed-form expression for capacitance of T-TSV

2.1. MOS effect

The T-TSV is filled with metal, and the Si substrate is doped. To electrically isolate the T-TSV from the conductive Si bulk, an
insulation layer (typically SiO$_2$) surrounding the T-TSV is necessary. Hence, a metal oxide semiconductor (MOS) structure is formed, as shown in Fig. 1. The T-TSV parasitic capacitance is similar to MOS field effect transistors under working condition, which can be referred to as “MOS effect”.

2.2. Capacitance of dielectric liner

The dielectric liner capacitance can be derived from the coaxial-cable capacitor model. Fig. 2 shows the geometric parameters of T-TSV, where $R_\text{m}$ and $R_\text{ox}$ are the bottom radii of the T-TSV metal and dielectric liner, respectively; $h$ is the height; $\theta_\text{ox}$ is the dielectric liner thickness; and $\alpha$ is the slope angle for the wall. T-TSV degenerates to cylindrical TSV when $\alpha=90^\circ$. Then, the top radii of T-TSV metal and dielectric liner can be expressed as $R_\text{m}+h\cot\alpha$ and $R_\text{ox}+h\cot\alpha$, respectively.

Applying Gauss’s law to T-TSV structure

$$\int_E ds = Q/e_\text{ox}$$

where $Q$ is the charge on the dielectric liner surface, $e_\text{ox}$ is the permittivity of dielectric liner. Since the thickness of oxide liner is generally very thin, the electric field $E$ can be assumed to be uniform. Hence, in Eq. (1), the integral is that of surface area. The electric field $E$ can be derived as

$$E = \frac{Q \sin \alpha}{e_\text{ox} \ln(2R_\text{ox}+h \cot\alpha)}$$  

The potential difference between the surfaces of dielectric liner $U_\text{ox}$ is given by

$$U_\text{ox} = \int_{R_\text{m}}^{R_\text{ox}} E dr = \frac{Q \sin \alpha}{2\pi e_\text{ox} h} \ln \left(\frac{2R_\text{ox}+h \cot\alpha}{2R_\text{m}+h \cot\alpha}\right)$$

The capacitance of dielectric liner can be obtained as

$$C_\text{ox} = \frac{Q}{U_\text{ox}} = \frac{2\pi e_\text{ox} h}{\sin \alpha \ln(2R_\text{ox}+h \cot\alpha)/(2R_\text{m}+h \cot\alpha)}$$

For $\alpha=90^\circ$, T-TSV degenerates to cylindrical TSV, Eq. (4) is simplified to

$$C_\text{ox} = \frac{2\pi e_\text{ox} h}{\ln(R_\text{ox}/R_\text{m})}$$

Eq. (5) coincides with the expression for the case of cylindrical TSV in [11].

2.3. Capacitance of depletion region

As has been mentioned, the MOS structure consists of TSV metal, dielectric liner, and Si bulk. The Si bulk is biased usually to ground potential. The signal in TSV corresponds to the bias voltage of MOSFET devices, and the conducting T-TSV metal acts as the gate electrode of a tapered MOS capacitor. A depletion region would emerge when the bias voltage is larger than flat-band voltage $V_{FB}$, as shown in Fig. 3. $R_\text{dep}$ represents the bottom radius of depletion region, which varies with working conditions. $R_\text{dep}$ has to be derived firstly by the following analysis before the depletion capacitance is obtained.

The full depletion approximation is used in this paper, which assumes that there are no mobile charge carriers in the depletion region. The applied TSV voltage drops across the dielectric liner and the Si bulk. Potential of Si bulk equals to the summation of $V_{FB}$ and the surface potential of dielectric liner, as given by

$$V_{TSV} = V_{FB} + \psi(R_\text{ox}) + U_\text{ox}$$

where $\psi(R_\text{ox})$ is the outside surface potential of dielectric liner; the flat-band voltage $V_{FB}$ is given by

$$V_{FB} = \phi_m - \phi_s - \frac{2\pi R_\text{ox} h Q_f}{C_\text{ox}} = \phi_m - \chi - \frac{E_g}{2}\ln\frac{N_s}{n_i} - \frac{2\pi R_\text{ox} h Q_f}{C_\text{ox}}$$

where $\phi_m$ and $\phi_s$ are the work function of T-TSV metal (typically Cu) and Si, respectively; $\chi$, $n_i$, and $E_g$ represent electron affinity, intrinsic carrier concentration, and band gap energy of Si, respectively; $q$, $N_s$, and $Q_f$ represent electronic charge, doping concentration of the acceptor ions and Si–SiO$_2$ interface charge density, respectively; the thermal voltage $V_T=KT/q$, $K$ is Boltzmann’s constant and $T$ is absolute temperature.

The charges on the metal $Q_m$ equal the ones in the depletion region, hence $U_\text{ox}$ from Eq. (6) can be written as

$$U_\text{ox} = \frac{Q_m}{C_\text{ox}} = \frac{q(N_s\pi(R_\text{dep}-R_\text{m}) \sin \alpha)}{2\pi e_\text{ox}} \ln \left(\frac{2R_\text{ox}+h \cot\alpha}{2R_\text{m}+h \cot\alpha}\right)$$

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The outside surface potential of dielectric liner $\psi(R_{ox})$ can be obtained by solving 2D Poisson’s equation in cylindrical coordinate system. Fig. 4 shows the cross-section view of T-TSV in cylindrical coordinate system.

The 2D Poisson’s equation is given by

$$\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \psi(r, z)}{\partial r} \right) + \frac{\partial^2 \psi(r, z)}{\partial z^2} = \frac{qN_2}{\varepsilon_{si}} (R_{ox} \leq r \leq R_{dep} + z \cot \alpha, 0 \leq z \leq h)$$

(9)

The dashed line in Fig. 4 represents a tapered surface of bottom radius $R$ ($R_{ox} \leq R \leq R_{dep}$), with slope wall parallel to the dielectric layer. The potential of this surface is represented by $\psi(R)$.

$$\psi(r, z) = \psi(R), \ (R = r - z \cot \alpha)$$

(10)

Thus the 2D Poisson’s equation degenerates to 1D situation

$$\frac{1}{R} \frac{\partial}{\partial R} \left( R \frac{\partial \psi(R)}{\partial R} \right) + \frac{qN_2}{\varepsilon_{si}} (R_{ox} \leq R \leq R_{dep})$$

(11)

where $\varepsilon_{si}$ is the permittivity of Si.

The boundary conditions given by Eqs. (12) and (13) suggest that the potential and electric field at the bottom of depletion region ($R_{dep}$) is zero.

$$\psi(R)|_{R = R_{ox}} = 0$$

(12)

$$\frac{\partial \psi(R)}{\partial R} |_{R = R_{dep}} = 0$$

(13)

The surface potential of the tapered surface with bottom radius of $R$ by solving the simplified 1D Poisson’s equation

$$\psi(R) = \frac{qN_2 R_{ox}^2}{4 \varepsilon_{si}} \min(R_{ox}) + \frac{qN_2 R_{dep}^2}{2 \varepsilon_{si}} \ln(R_{dep} - 1)$$

(14)

Then the outside surface potential of dielectric liner $\psi(R_{ox})$ can be obtained by substituting $R_{ox}$ for $R$. $R_{dep}$ can be derived by putting Eqs. (6)–(8) and (14) together. Similar to the dielectric liner, the capacitance of depletion region can be given as

$$C_{dep} = \frac{2 \pi \varepsilon_{si} h}{\sin \alpha \ln(2R_{ox} + h \cot \alpha)/(2R_{ox} + h \cot \alpha)}$$

(15)

2.4. Threshold voltage ($V_{th}$) and minimum depletion capacitance ($C_{dep min}$)

The threshold voltage of T-TSV ($V_{th}$) is defined as the TSV voltage at which the Si–SiO$_2$ surface potential equals 2$V_T$ $\ln(N_2/N_1)$. When the bias voltage of T-TSV reaches $V_{th}$, the depletion capacitance is at its minimum value $C_{dep min}$.

$$\frac{qN_2 (R_{ox}^2)}{4 \varepsilon_{si}} - \frac{qN_2 R_{max}^2}{2 \varepsilon_{si}} \min(R_{ox}) + \frac{qN_2 R_{dep}^2}{2 \varepsilon_{si}} [2 \ln(R_{max}) - 1] = 2V_T \ln \frac{N_2}{N_1}$$

(16)

where $R_{max}$ represents the maximum bottom radius of depletion region, and can be obtained by solving Eq. (16). We can solve Eqs. (5) and (16) simultaneously for the threshold voltage $V_{th}$

$$V_{th} = V_{FB} + 2V_T \ln \frac{N_2}{N_1} + \frac{qN_2 \pi (R_{max}^2 - R_{ox}^2)}{2 \pi \varepsilon_{ox}} \sin \alpha \ln \left( \frac{2R_{ox} + h \cot \alpha}{2R_{max} + h \cot \alpha} \right)$$

(17)

Substituting $R_{max}$ for $R_{dep}$ in Eq. (15), the minimum depletion capacitance $C_{dep min}$ can be given as

$$C_{dep min} = \frac{2 \pi \varepsilon_{si} h}{\sin \alpha \ln(2R_{ox} + h \cot \alpha)/(2R_{ox} + h \cot \alpha)}$$

(18)

2.5. Closed-form capacitance model of T-TSV considering MOS effect

The total capacitance of T-TSV $C_{TSV}$ is the series combination of the dielectric liner capacitance and depletion capacitance. According to the description all above, the closed-form expression for the capacitance of T-TSV considering MOS effect is given by

$$C_{TSV} = C_{ox} = \frac{2 \pi \varepsilon_{ox} h}{\sin \alpha \ln(2R_{ox} + h \cot \alpha)/(2R_{ox} + h \cot \alpha)}$$

(19)

Region B. Depletion Region ($V_{FB} \leq V_{TSV} < V_{th}$)

$$C_{TSV} = (C_{ax} - 1 + C_{dep min})^{-1} = \left[ \frac{1}{2 \pi \varepsilon_{si} h} \sin \alpha \ln \left( \frac{2R_{ox} + h \cot \alpha}{2R_{max} + h \cot \alpha} \right) \right]^{-1}$$

(20)

Region C. Minimum Capacitance Region ($V_{TSV} \geq V_{th}$)

$$C_{TSV} = (C_{ax} - 1 + C_{dep min})^{-1} = \left[ \frac{1}{2 \pi \varepsilon_{si} h} \sin \alpha \ln \left( \frac{2R_{ox} + h \cot \alpha}{2R_{max} + h \cot \alpha} \right) \right]^{-1}$$

(21)

For $\alpha = 90^\circ$, Eqs. (19)–(21) degenerates to

$$C_{TSV} = C_{ax} = \frac{2 \pi \varepsilon_{ax} h}{\ln(R_{ox}/R_{min})}$$

(22)

Region B. Depletion Region ($V_{FB} \leq V_{TSV} < V_{th}$)

$$C_{TSV} = \left[ \left( \frac{\ln(R_{ox}/R_{min})}{2 \pi \varepsilon_{ax} h} \right) + \left( \frac{\ln(R_{max}/R_{min})}{2 \pi \varepsilon_{ax} h} \right) \right]^{-1}$$

(23)

Region C. Minimum Capacitance Region ($V_{TSV} \geq V_{th}$)

$$C_{TSV} = (C_{ax} - 1 + C_{dep min})^{-1} = \left[ \left( \frac{\ln(R_{ox}/R_{min})}{2 \pi \varepsilon_{ax} h} \right) + \left( \frac{\ln(R_{max}/R_{min})}{2 \pi \varepsilon_{ax} h} \right) \right]^{-1}$$

(24)

Expressions (22)–(24) coincide with the case of cylindrical TSV in [12].

3. Verification and discussion

The closed-form expression for the capacitance of T-TSV proposed above is verified by employing ANSYS Q3D Extractor. The Si–SiO$_2$ interface charge density $Q_i/q$ is $5 \times 10^{10}$ cm$^{-2}$; $N_2$ is 1.25 x 10$^{15}$ cm$^{-3}$; the bottom radius and height of T-TSV are 2.5 μm and 10 μm respectively; and 0.1 μm thick dielectric liner is used around the T-TSV.

Fig. 5(a) compares the parasitic capacitance results based on the closed-form expression and the ANSYS Q3D Extractor simulation in [12].
the cases of $\alpha = 75^\circ$, $80^\circ$, $85^\circ$ and $90^\circ$. It is observed that, the capacitance got by the closed-form expression produces a less than 5% error difference from ANSYS Q3D Extractor simulation results, indicating that (4) is highly precise. It is also found from Fig. 5(a) that, the parasitic capacitance is invariant in the accumulation region (region A). When the bias voltage is larger than flat-band voltage (region B), the capacitance decreases due to the decreasing depletion capacitance. When the bias voltage is larger than threshold voltage (region C), the capacitance reaches the minimum value, and maintains invariant again. This acts as MOS devices. The maximum and minimum capacitances are 76 fF and 23 fF, respectively. The flat-band line and threshold line in Fig. 5(a) point out respectively the flat-band voltage and threshold voltage for all the cases. The capacitance decreases as the slope wall angle ramps up, due to the decreasing area of the coaxial-cable capacitor.

Fig. 5(b) gives the errors in neglecting MOS effect. The error increases with the increasing bias voltage in region B. In region C, the error reaches 225%, which proves MOS effect indispensable in the parasitic capacitance model of T-TSV.

Next, taking slope wall angle of $80^\circ$ for instance, the capacitance characterization of copper T-TSV is discussed using the presented model. The dielectric liner capacitance $C_{ox}$, the depletion capacitance $C_{dep}$ and the total capacitance of T-TSV $C_{TSV}$ are also analyzed. The capacitance of region A is equal to $C_{ox}$ of regions B and C, so the following analysis does not contain the cases of region A. The voltages of 0.5 V and 1 V are biased on the T-TSV for regions B and C, respectively.

Fig. 6 gives the variations of $C_{ox}$, $C_{dep}$ and $C_{TSV}$ with $R_m$. It shows that all the capacitances increase linearly with the increasing $R_m$, due to the linearly increasing area of the coaxial-cable capacitor.

$C_{ox}$ is affected more significantly than $C_{dep}$ by the increasing $R_m$, which can be explained by the fact that the thickness of depletion region (about 0.6 $\mu$m) is 6 times that of dielectric liner, but the permittivity of depletion region is only 3 times the liner dielectric constant. The total capacitances of regions B and C increase by about 25 fF.

Fig. 7 shows the variation of parasitic capacitance with dielectric liner thickness $t_{ox}$. Apparently, $C_{ox}$ decreases with increasing $t_{ox}$. Both of the depletion capacitances increase with increasing $t_{ox}$, which is because the thicker the dielectric liner, the thinner the depletion region for region B and the larger the surface area. The total capacitances of both regions B and C decrease by about 12 fF.

Fig. 8 shows the variations of $C_{ox}$, $C_{dep}$ and $C_{TSV}$ with different dielectric liner materials. It is observed that $C_{ox}$ increases linearly with the increasing liner dielectric constant. Under the same working condition for region B, the larger the liner dielectric constant, the thicker the depletion region, which results in a decreasing $C_{dep}$. The depletion capacitance of region C does not change due to the invariable depletion region. The total capacitances of both regions B and C increase by about 12 fF.

Fig. 9 shows the change of parasitic capacitance with T-TSV height. It is observed that the total capacitances of both regions B and C increase by about 210 fF. All the parasitic capacitances increase with the increasing T-TSV height, because the higher the T-TSV, the larger the area of the coaxial-cable capacitors.

Fig. 10 gives the variation of parasitic capacitance with the acceptor concentration. It can be seen that the acceptor concentration has no influence on $C_{ox}$. Both the depletion capacitances increase with the increasing acceptor concentration. This happens because the
Applying Gauss’s law to the cylindrical TSV structure, the dielectric liner capacitance can be derived as
\[ C_{ox,c} = \frac{2\pi e_{ox} h}{\ln(2R_{ox} + h \cot \alpha)/(2R_{ox} + h \cot \alpha)} = C_{ox,T} \sin \alpha \]  
(25)

where the subscripts \( C \) and \( T \) represent cylindrical TSV and T-TSV, respectively. Since the impact of \( \alpha \) on \( R_{dep} \) is negligible, the depletion capacitance can be given similarly
\[ C_{dep,c} = \frac{2\pi e_{ox} h}{\ln(2R_{dep} + h \cot \alpha)/(2R_{dep} + h \cot \alpha)} = C_{dep,T} \sin \alpha \]  
(26)

Therefore, the relationship between the total capacitances of cylindrical TSV and T-TSV can be obtained
\[ C_{TSV,T} = C_{TSV,T} \sin \alpha \]  
(27)

\( \Delta E \) stands for the acceptable relative error. If \( 1 - \sin \alpha > \Delta E \), i.e., \( \alpha < \arcsin(1 - \Delta E) \), it would be recommended to use the sloped TSV formula instead of a cylindrical approximation. For example, assuming \( \Delta E = 5\% \), the critical angle is 73°.

5. Conclusion

In this paper, firstly, MOS effect is introduced, and closed-form expression for the parasitic capacitance of T-TSV is proposed by solving 2D Poisson’s equation based on the capacitance models of the dielectric liner and depletion region. When slope wall angle is 90°, the expression is simplified and coincides with the one reported for cylindrical TSV. Secondly, by employing ANSYS Q3D Extractor, the expression is verified. A less than 5% error is shown for \( \alpha = 75°, 80°, 85° \) and 90°; when MOS effect is ignored, the error reaches 225%, which proves MOS effect indispensable to the analytical model. Thirdly, the parametric study is performed on the capacitance of copper T-TSV with slope wall angle of 80°. The results show that the capacitance of T-TSV acts as that of MOS device in changing the bias voltage. The increase in the bottom radius of T-TSV (from 1 to 5 \( \mu \)m), dielectric liner thickness (from 0.1 to 0.5 \( \mu \)m), liner dielectric constant (from 1 to 5), height of T-TSV (from 10 to 50 \( \mu \)m), and acceptor concentration (from \( 1 \times 10^{15} \) to \( 5 \times 10^{15} \) cm\(^{-3} \)) cause the increase in T-TSV capacitance by about 25 \( \mu \)F, 12 \( \mu \)F, 12 \( \mu \)F, 210 \( \mu \)F and 12 \( \mu \)F, respectively. The parasitic capacitance of T-TSV can be changed in order to meet the circuit demand by adjusting the parameters analyzed in this paper. Finally, the condition for T-TSV simplified to cylindrical TSV is obtained. This paper provides an important theoretical basis for 3D IC reliability and flexibility design.

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