A COMPARATOR-BASED SWITCHED-CAPACITOR INTEGRATOR USING A NEW CHARGE CONTROL CIRCUIT

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ABSTRACT
A comparator-based switched-capacitor (CBSC) integrator is presented. In contrast to an opamp-based switched-capacitor (OBSC) circuit, a comparator-based switched-capacitor circuit needs an extra circuit to control the charge flow in the charge transfer phase. A new charge control circuit is proposed to control the charge transfer phase of a CBSC integrator. In comparison to the existing charge control scheme, the proposed charge control scheme makes the output settling faster.

I. INTRODUCTION
Today most switched-capacitor based applications use an opamp for operation. Opamp gain is an important factor for the accuracy of these kinds of circuits [1]. However, the technology scaling places some constraints on the opamp gain and output swing. Several solutions with delicate trade-offs have been invented so far to reduce the effects of technology scaling on opamp design.

Recently, a new methodology [2] has been reported which uses a comparator with current sources at its output instead of an opamp in sampled data systems. The idea is based on the detection of a virtual ground condition rather than forcing it via feedback. The advantages to this approach are inherently higher power efficiency, a removal of feedback and stability concerns, and its compatibility to most known opamp based architectures. On the other side, only switched-capacitor loads can be driven [3]. A pipeline ADC using a single ended CBSC gain stage [2] and a delta-sigma modulator using a pseudo-differential CBSC gain stage [3] have been fabricated so far. In addition, the transient noise in CBSC circuits has been analyzed in [4].

In contrast to an OBSC circuit, in a CBSC circuit, there is no virtual ground condition at the comparator inputs; therefore, an extra circuit is needed to detect the virtual ground condition using the comparator output and control the charge flow in the charge transfer phase accordingly. In this paper, we have proposed a new charge transfer scheme and the related circuit which makes the charge transfer phase faster. In section II, the current approach to control the charge transfer phase and our new charge control scheme are explained. In section III, the circuit which realizes this new charge control scheme is illustrated. Simulation results for a typical integrator are presented in section IV.

II. CBSC CHARGE TRANSFER SCHEMES
The CBSC technique is illustrated in Fig. 1. The integrator in Fig. 1 uses a comparator with two current sources at its output instead of an opamp. The circuit operates in two phases. In the sampling phase (Q₂), C₂ is charged by input (this phase is not shown in Fig.1). At the beginning of the charge transfer phase (Q₁) a brief preset (P) of the stage must be done to clear C_L and ensure Vₓ starts below the common mode voltage (V_CM). The preset is done by momentarily pulling the output node to the lowest potential in the system (VSS). Next the coarse charge transfer phase (E₁) begins. Current source I₁ results in a relatively fast voltage ramp on Vₓ toward V_CM. At this point, the comparator makes its first decision. Because the comparator has a finite delay, I₁ turns off after Vₓ crosses V_CM. After I₁ turns off, current sink I₂ turns on to begin the fine charge transfer phase (E₂). The current I₂ is less than I₁ and results in a slower ramp back toward V_CM. When the ramp at Vₓ crosses V_CM again, the sampling switch (S) is opened after the brief delay of the comparator. The correct charge is sampled on C_L at that moment. The final overshoot from the comparator delay is a constant offset in the output if
the ramp rate and the comparator delay are constant [2].

We have proposed another charge transfer scheme which does not need any preset of the output node at the beginning of the charge transfer phase, because here it is not necessary for \( V_X \) to start below the comparator input common mode voltage (\( V_{CM} \)). The proposed approach and its timing diagram are depicted in Fig. 2. In this approach, at the beginning of the charge transfer phase, based on the voltage \( V_X \), the current source \( I_1 \) or the current sink \( I_2 \) will turn on to begin the coarse charge transfer phase (\( E_1 \)). As soon as \( V_X \) crosses \( V_{CM} \), the active current source (\( I_1 \) or \( I_2 \)) will turn off and the fine charge transfer phase will start by turning either \( I_3 \) or \( I_4 \) on. The current \( I_3 \) and \( I_4 \) are less than \( I_1 \) and \( I_2 \) and result in a slower ramp back toward \( V_{CM} \). The fine charge transfer phase will finish as soon as \( V_X \) crosses \( V_{CM} \) again and the active current source (\( I_3 \) or \( I_4 \)) will then turn off. When all the current sources and the current sinks are inactive, the output node will be floating; therefore, the charge on \( C_L \) will not change.

Eliminating the need to preset the output node at the beginning of the charge transfer phase will result in faster output settling. That is because the output node is not forced to start being charged from \( V_{SS} \) in each clock cycle so less charge and consequently less time is needed to make output.

III. PROPOSED CHARGE CONTROL CIRCUIT

In this part, we first introduce a single ramp charge control circuit (i.e. the coarse charge transfer phase will only occur) and then we extend it to a dual ramp one. For practical applications a dual ramp charge control circuit is more desirable because the final overshoot due to the comparator delay will be negligible.

The proposed charge control circuit consists of two parts. The first part is a logic circuit which controls the current sources and the current sinks. The second part is a current drive circuit which is made of a current source and a current sink (two current sources and two current sinks for the dual ramp charge control circuit) and is controlled by the output of the control logic circuit and the output of the comparator. Fig. 3 shows how this charge control circuit is used in an integrator. The control logic circuit and the current drive circuit for a single ramp charge control circuit are shown in Fig. 4 and Fig. 5 respectively.

In phase \( Q_2 \), \( C_1 \) will be charged by \( V_{IN} \). When phase \( Q_1 \) begins, the comparator will make decision based on the voltage difference at its inputs. \( V_{CMP-OUT} \) is the comparator output. The clock signal \( Q_1 \) is connected to a positive edge triggered D-Flip-Flop which will store the comparator output as soon as it is available; therefore, the DFF must wait until the comparator makes its decision. That is why the first delay block is used (Fig. 4). The DFF output and the comparator output are connected to an XNOR gate which will finally make a low output level at \( V_{CONTROL} \). The second delay block is used to take the DFF and the XNOR propagation delay into account. The final low level at \( V_{CONTROL} \) will turn on the current drive circuit. The current drive circuit determines to turn on the current source or the current sink based on the comparator output. The current drive circuit is discussed later in this section. After that the current source or the current sink is activated it will start charging or discharging the capacitors. The comparator output will change as soon as \( V_X \) crosses \( V_{CM} \). This will change the output of XNOR which will finally make \( V_{CONTROL} \) high. This will turn off the current drive circuit. At this point the correct charge is sampled on \( C_L \). The clock signal is also connected to the NAND gate directly. This is to disable the current drive circuit as soon as phase \( Q_1 \) ends (otherwise the signal \( Q_1 \) must pass through the delay blocks to disable the
current drive circuit, and meanwhile, the comparator output may change as soon as Q₁ is disabled and this may turn the current drive circuit on again).

Fig. 5 shows the current drive circuit. \( I_{\text{REF}} \) provides the reference current for the current source (M₁ and M₃ current mirror) and the current sink (M₂ and M₄ current mirror). M₅–M₈ are switches which are used for turning the current source or the current sink, on or off, based on the comparator output (\( V_{\text{CMP-OUT}} \)) and the control logic circuit output (\( V_{\text{CONTROL}} \)). When \( V_{\text{CONTROL}} \) is high, both current mirrors will be off regardless of \( V_{\text{CMP-OUT}} \). When \( V_{\text{CONTROL}} \) is low, \( V_{\text{CMP-OUT}} \) determines which current mirror will be active. In this case, if \( V_{\text{CMP-OUT}} \) be high, the current source (M₁ and M₃ current mirror) will be active, otherwise the current sink (M₂ and M₄ current mirror) will be active.

The control logic circuit and the current drive circuit for a dual ramp CBSC integrator are shown in Fig. 6 and Fig. 7 respectively. The control logic circuit has changed a little. A negative edge triggered JK-Flip-Flop and two NAND gates are added (Fig. 6) to make the required control signals for the current drive circuit. The JKFF will be reset in phase Q₂. When phase Q₁ begins, on the first negative edge of \( V_C \), the JKFF will toggle, so \( V_{\text{CON1}} \) will go low and as a result the coarse charge transfer phase (\( E_1 \)) will start. \( V_C \) will change as soon as \( V_X \) crosses \( V_{\text{CM}} \) (Fig. 2), so \( V_{\text{CON1}} \) will go high and \( V_{\text{CON2}} \) will go low. Consequently, phase \( E_1 \) will finish and the fine charge transfer phase (\( E_2 \)) will start. \( V_C \) will change again and it will make a negative edge transition as soon as \( V_X \) crosses \( V_{\text{CM}} \) again. This will make JKFF toggle and both control signals, \( V_{\text{CON1}} \) and \( V_{\text{CON2}} \), will go high. As a result, the current drive circuit will become inactive. At this moment the correct charge is sampled on \( C_L \).

If we look at the comparator together with the charge control circuit as a single block then the output of this block is active during Q₁ and it is...
inactive during Q2 as in the case of switched-opamp circuits [5]. So it seems that this block can be placed instead of opamps in switched-opamp based circuits without any major changes.

IV. SIMULATION RESULTS

In order to test the charge control circuit, it was used in an integrator similar to Fig. 3. The input was a sinusoidal signal with a frequency of 100 KHz and the amplitude of 100 mV. The clock frequency was 1 MHz. C1 and C2 were chosen 1 pF and 2 pF respectively. A continuous time voltage comparator was used in our design (Fig.8). It consists of a preamplification stage (M1 – M7), a decision stage (M8 – M12), and an output buffer (M13 – M20) [6]. M12 is biased in triode region and acts to shift the output level of the decision circuit upward to be in the common mode range of the output buffer. The comparator input offset voltage was 1mV.

The voltages across C1 and C2 for the single ramp and the dual ramp CBSC integrators are shown in Fig. 9 and Fig. 10 respectively. The final offset error due to the finite comparator delay was about 16 mV for the single ramp CBSC integrator and about 2 mV for the dual ramp one.

Digital parts are realized in static CMOS logic. The delay blocks can be realized by cascading some inverters, or delayed clock signals can be used instead. We cascaded some inverters to make delay blocks. All digital parts use transistors with minimum feature size; therefore, the overhead due to the digital parts is negligible. All circuits including digital and analog, use a 1.5v power supply voltage. The comparator input common mode voltage was set to the middle of the supply voltage. In our design, the comparator limits the minimum power supply voltage; therefore, the power supply voltage can be further reduced if a low-voltage comparator is used. The circuits are designed in a 0.18 µm CMOS technology. Both PMOS and NMOS transistors have a threshold voltage equal to 0.5v. HSPICE was used for simulation.

CONCLUSION

A CBSC integrator was presented with a new charge control scheme. The new charge control scheme compared to the conventional one is inherently faster because it does not require the output node to be preset to VSS in each clock cycle; therefore, the output signal can settle faster.

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REFERENCES