Envelope Tracking Pulse Gate Modulated GaN HEMT Power Amplifier for Wireless Transmitters

Maryam Jouzdani, Student Member, IEEE, Mohammad Mojtaba Ebrahimi, Member, IEEE, Karun Rawat, Senior Member, IEEE, Mohamed Helaoui, Member, IEEE, and Fadhel M. Ghannouchi, Fellow, IEEE

Abstract—This paper proposes a complete transmitter prototype for wireless applications using envelope tracked pulse gated modulated power amplifier (PA). The proposed transmitter architecture is developed using two high power 10 W gate modulated PAs combined in a fashion to operate as a switched voltage source for the range of duty cycles of pulses driving the gates of power amplifiers. These PAs are designed and implemented using packaged GaN HEMT transistors from CREE to operate at the carrier frequency of 2.35 GHz. For a 5 MHz bandwidth WiMAX 802.16c down-link signal with the PAPR of 7.9 dB and the oversampling ratio of 100, the average drain efficiency of 46.2% is achieved at the average output power of 35.8 dBm. Using a 5 MHz bandwidth LTE down-link signal with 11 dB PAPR and centered at 2.35 GHz, the power amplifier delivers the average output power of 33.2 dBm with the average drain efficiency of 46%. The adjacent channel leakage ratio (ACLR) measured for this signal is less than –36.85 dBc at 10 MHz offset from the center frequency of 2.35 GHz.

Index Terms—Delta-sigma modulation, Doherty power amplifier, field-programmable gate array (FPGA), GaN HEMT, Long Term Evolution (LTE), peak-to-average power ratio, power amplifier, quantization noise, Worldwide Interoperability for Microwave Access (WiMAX).

I. INTRODUCTION

RECENT advances in modern wireless communications have introduced mobile standards such as 3GPP LTE, 4G LTE-Advanced, and WiMAX to provide high speed data access services for all users [1]. These standards utilize orthogonal frequency division multiplexing (OFDM) as a modulation scheme. Transmitting OFDM modulated signals with non-constant envelopes and high PAPRs necessitates using power amplifiers with high power efficiency at the output power back-off (OPBO) region. Techniques such as envelope elimination and restoration (EER) [2]–[4], envelope tracking (ET) [5]–[7], Doherty [8]–[11] and Chireix outphasing [12]–[15] have been reported for the purpose of improving the power amplifier’s efficiency while maintaining the required linearity. Well-known PA configurations such as Doherty PA (DPA) and the Chireix outphasing amplifier use load modulation technique and some other structures like EER and ET transmitters benefit from the supply modulation techniques to improve the power efficiency. In Doherty PA design, for instance, the main amplifier’s output load impedance is modulated at the back-off operation by applying a class-C amplifier (peaking amplifier) as a current source.

In the EER and the envelope tracking transmitter configurations, the average efficiency of the power amplifier improves by modulating the supply voltage of the RF PA. The operating principle of the EER transmitter is to split the phase and envelope information of the input modulated signal by sending the input signal to a limiter and an envelope detector, respectively. The supply voltage of the amplifier is then modulated by the envelope of the modulated signal through an efficient envelope amplifier so that the power amplifier operates close to the saturation region for all envelope amplitudes. Although these techniques promise optimal efficiency over any power levels, design of linear, high efficient envelope amplifier is challenging for EER and ET transmitters. Recently, pulsed modulated modified polar transmitters have been reported in [16]–[18] to remove the envelope amplifier from the drain supply path of the RF amplifier. In these architectures, the signal’s envelope is encoded to a pulse train, using a pulse width modulator (PWM), and then the envelope pulse train controls a mixer or a switch at the gates of nonlinear, high efficient RF power amplifiers.

The supply modulation of the power amplifier can be in terms of the drain or the gate bias. In particular, if the gate bias of PA is driven by digital pulses, the PA with pulse gate modulation must operate like a switched voltage source with different duty cycles of pulses, in order to amplify efficiently. One such scheme, is based on the digital load modulation technique named pulsed load modulation (PLM) was recently introduced to improve the power efficiency of PAs at the 6 dB OPBO region [19]. In 2010, a PLM power amplifier was designed based on GaAs pHEMT devices for the maximum output power of 27.1 dBm [20].

This paper presents a complete transmitter architecture inspired by the PLM technique, where, the two high power GaN HEMT PAs are connected as in Doherty PA fashion to operate in envelope gate modulation (EGM) scheme. The block diagram of power amplifiers used for the proposed transmitter architecture is shown in Fig. 1. The main and auxiliary amplifiers are controlled through their gate biases by digital pulses generated from one bit envelope modulator such as the envelope delta-sigma modulator (DSM). The input signal of the EGM amplifier is the carrier modulated phase of the signal with a constant envelope.

As shown in Fig. 1, the main and auxiliary amplifiers are connected together by a 90° transmission line and they are switched at the same time by the modulated envelope of the signal between the class-B (the on state) and pinch-off (the off state). A
driver is used at the input of the amplifier to provide better isolation and to prevent the input phase modulated carrier signal from leaking to the output during the off state. Digital load modulation behavior of the power amplifier is based on the switched resonator performance. Digital load modulation technique forces both main and auxiliary amplifiers to operate in the voltage saturation mode in the 6 dB power back off region. Therefore, unlike DPA, the average efficiency of the ideal pulsed gate modulated amplifier stays at its maximum value for up to 6 dB back-off from the peak output power.

In this paper for the first time, an EGM transmitter prototype based on 10 W GaN HEMT transistors is designed and implemented for efficient wireless applications. The transmitter prototype is developed by implementing a high power EGM power amplifier. In order to design the EGM PA for high power applications, a proper strategy is required to switch the devices on and off with gate pulses. In the proposed scheme, a proper strategy has been implemented to condition gate pulses in order to switch 10 W GaN devices at high speed. A level shifter interface circuit is designed and fabricated to change the voltage levels of the pulses generated from the FPGA to the levels that can switch the amplifiers between the on states and off states. The switching characteristics of the EGM technique makes it essential to use wide band gap devices in order to design main and auxiliary amplifiers. Good efficiency, high power handling and high drain-gate breakdown voltages of the GaN HEMT transistor make this device a good candidate for the design of high power EGM power amplifier. For experimental verification, the transmitter setup is tested by practical standards’ signals with various PAPRs. The envelope of the original signal is digitized by a 1-bit second order EDSM using a high speed Altera FPGA. The constant envelope modulated signal is then transmitted to the gate biases of the main, auxiliary and digital driver amplifiers through level-shifter interface circuits. The phase of the signal is up-converted to the carrier frequency through a wideband I/Q modulator. The RF modulated phase goes to the input of the digital driver and then is fed to the input of the PA. A high Q bandpass filter (BPF) is placed at the output of the power amplifier to remove the quantization noise caused by the envelope modulator from the output signal.

This paper is organized as follows. Section II gives a brief overview on the load modulation behavior in EGM PAs and presents the design procedure of the EGM power amplifier. The design and implementation of a 10 W GaN pulsed gate modulated PA for base-station applications are explained in Section III. Section IV presents the complete fabricated prototype of the transmitter, including its digital base-band setup, the power amplifier, and the output BPF. The setup is tested initially with square pulses with various duty cycle values and then with several practical standards’ signals and the results are presented in Section V.

II. PRINCIPLES OF OPERATION AND THEORY

Digital load modulation of the pulsed gate modulated power amplifier is based on dynamic load variations in switched resonator [20]–[23]. This section presents the load modulation characteristics of the EGM amplifier in more details. Fig. 2 shows a typical switched resonator circuit with a series LC tank. A switched resonator consists of a switched controlled RF source, a high Q resonator (or bandpass filter) tuned at the frequency of the RF input signal, terminated with a load. The energy stored in the resonator is controlled by the switching action speed so that variable impedance behavior can be obtained at the input of the resonator. If the switching action happens with a switching period (T) shorter than the time constant of the resonator and with a switching frequency less than the RF signal frequency (fc), the resonator’s input impedance is determined by the duty cycle (D) of the pulses, which can be written as [20]:

\[
R_{eff} = \begin{cases} \frac{1}{D} \frac{V_{in}}{I_{in}} & 0 \leq t < D \cdot T \\ \frac{1}{D} \frac{V_{opt}}{R_{opt}/2} & D \cdot T \leq t < T \end{cases}
\]  

(1)

where \(I_{in}\) is the current of the load terminal and \(R_{opt}\) is the optimum matching impedance of a Class-B amplifier that will be discussed later in this section. As a result of the short switching period, the energy stored in the resonator and the output voltage waveform can be approximately considered as a constant within each period. The output voltage and current can be expressed as:

\[
V_{out} = DVA,
\]

(2)

\[
I_{out} = \frac{V_{out}}{R_{L}} = \frac{DVA}{R_{opt}/2} = 2DI_{max}.
\]

(3)

and therefore, the output power at the load level can be calculated as:

\[
P_{out} = \frac{1}{2}I_{out}V_{out} = \frac{1}{2}(2DI_{max})(DVA) = D^2I_{max}VA.
\]

(4)

From (1) and (4) it can be seen that in a switched resonator circuit, the load impedance at the input of the resonator and
the output power can be controlled by the duty cycles of the switching pulses.

To verify the load modulation characteristics of the switched resonators, an envelope simulation is done using Advanced Design System (ADS) software (Agilent Technologies) for an ideally switched high Q series LC resonator tuned at the frequency of 10 MHz and with the load impedance of 25 ohm. The switch action is made using pulses with pulse repetition frequency (PRF) of 10 MHz and various duty cycles (D = 10% to 90%). As shown in Fig. 3, the input impedance of the resonator changes inversely with the duty cycle of the pulse.

The efficiency enhancement method in the EGM amplifier is derived from the idea of the load modulation in series LC switched resonators. In the EGM PA, the auxiliary amplifier can be modeled like a voltage source during the on state such as in switched resonators since it is forced to operate in the saturation mode. When the gate pulses are low, both amplifiers are off and the high output impedance of the main amplifier is transformed into a virtual ground at the input of the bandpass filter through the 90° transmission line. If the switching action happens faster than the bandwidth of the output filter, the effective input impedance of the filter (Reff) varies inversely with the duty cycle of the gate-bias pulses. Consequently, it can be shown that the output power is proportional to the square of the duty cycle of the switching pulses during the on state and the optimal efficiency performance can be achieved.

The performance of the EGM amplifier can be analyzed and tested using variable duty cycle pulses as gate biases for both main and auxiliary PAs. For pulses with duty cycles less than 50%, the output power back off level is more than 6 dB. The input power division between the main and auxiliary amplifiers (Rmain and Raux) for variable duty cycles.

\[
\eta_{PA} = \frac{P_{out}}{P_{DC}} = \frac{D^2 I_{max} V_{max}}{I_{DC-Main} V_{DC-Main} + I_{DC-Aux} V_{DC-Aux} - \frac{D^2 I_{max} V_{max}}{2}} \quad 0 \leq D \leq 50\%
\]

in which \( V_{max} \) equals to the drain supply voltage of the class-B amplifier. As the duty cycle of the switched pulses increases from 50% to 100%, in the 6 dB OPBO region, the main amplifier provides \( I_{max} \) to the output load and the auxiliary amplifier starts providing the remaining current to the load as its output impedance reduces due to the load modulation behavior of the EGM amplifier. At full power level, both amplifiers contribute equally in delivering the maximum current of 2\( I_{max} \) to the load.

\[
\eta_{PA} = \frac{D^2 I_{max} V_{max}}{(2-D)(I_1 + I_2) V_{max}} \quad 50\% \leq D \leq 100\%
\]

Therefore, the drain efficiency of the EGMPA designed with two class-B amplifiers at 6 dB OPBO region can be written as:

\[
\eta_{PA} = \frac{D^2 I_{max} V_{max}}{(\frac{2}{\pi} D)(I_{max} + (2D-1)I_{max}) V_{max}} \quad 50\% \leq D \leq 100\%.
\]

Since both amplifiers stay in saturation at 6 dB OPBO region, the efficiency of the EGM PA stays at the optimum value (around 78%) for ideal class-B amplifiers [20]. Fig. 4 shows the theoretical drain efficiency of the PA along with the load impedances seen at the output of the main and auxiliary amplifiers (\( R_{main} \) and \( R_{aux} \)) for different duty cycle values. In this analysis, the optimum load impedance of the main and auxiliary amplifiers (\( R_{opt} \)) is supposed to be 50 ohm. The load impedance seen at the combination point of the main and auxiliary amplifiers (\( R_{eff} \)) is also plotted in Fig. 4. It can be seen in this figure that the load impedance \( R_{eff} \) varies inversely with the duty cycle values.

III. DESIGN AND SIMULATION OF GaN BASED PULSE GATE MODULATED PA

To validate the efficiency performance of the EGM amplifier, an EGM PA is designed and simulated at 2.35 GHz using Agilent ADS software harmonic and envelope simulators. Two class-B amplifiers are designed with satiability circuits and input/output matching networks utilizing two 10 W GaN HEMT transistor device models from Cree (CGH40010F) as the main and auxiliary amplifiers. An uneven 90° branch line hybrid coupler has been used as a power divider at the input of the EGM PA to drive the main amplifier with slightly more...
power than the auxiliary amplifier [24]. The power divider is designed to have a bandwidth of 280 MHz around the center frequency. The main and auxiliary amplifiers are connected together at their output by a 90° transmission line. To investigate the amplifier efficiency performance, in this simulation, an ideal high Q BPF model centered at the frequency of 2.35 GHz is utilized before the output load. A λ/4 transmission line with characteristic impedance of 35 ohm is placed between the combination points of two amplifiers in the PA structure and the output filter.

Pulse trains with the pulse repetition frequency of 100 MHz are used to switch both main and auxiliary amplifiers simultaneously between the class-B and deep pinch-off region through their gate-source biases. Duty cycles of the gate-bias pulses are varied from 0% to 90% in this simulation. A digital driver is designed for the input of the amplifier to provide better isolation and to prevent the input phase modulated carrier signal from leaking to the output during the off state. In this simulation, a single tone signal at RF frequency of 2.35 GHz is the input of the driver and the PA. In order to compare the efficiency performances of the EGM PA with the Doherty PA and the balanced class-B amplifiers, these PAs are designed using 10 W GaN transistors. Fig. 5 shows the theoretical efficiency of the EGM PA (normalized to the achievable efficiency in simulation at peak power) and the average drain efficiency of the simulated EGM amplifier with ideal filtering at the PA’s output. For better comparison, the drain efficiency of a Doherty PA and a balanced class-B PA are also shown in Fig. 5. As illustrated in Fig. 5, the average drain efficiency of the designed EGM amplifier is higher than 61.4% in simulation and it is almost flat in the 6 dB power back off region unlike the Doherty PA.

IV. GaN EGM Based Transmitter Prototype

Fig. 6 displays the block diagram of the proposed GaN based envelope gate modulated transmitter. It includes the digital baseband blocks to generate the delta-sigma modulated signal from the signal’s envelope and IQ signals from the signal’s phase, level-shifter interface circuits to suitably adjust the transistors’ gate signals, an I/Q modulator to up-convert the phase signal to the carrier frequency, the digital driver, the EGM PA, and the output thigh Q bandpass filter.

A. GaN HEMT Transistor EGM PA Fabrication

The PA is implemented using two packaged 10 W GaN HEMT transistors from Cree Inc., Durham, NC, USA. The circuit is fabricated on Rogers RT/duroid 5870 board with the thickness of 20 mil. Fig. 7 shows the photograph of the fabricated EGM PA with the input power divider. The total size of implemented EGM circuit is approximately 4.7” × 3.3”. The main and auxiliary amplifiers are biased at class-B and the dc supply voltages at their drain terminals are set to 28 V. The gate biases are maintained constant throughout the first experiment.

The PA is tested with a single-tone continuous wave excitation as the input signal at the center frequency of 2.35 GHz and with variable power levels. The measured drain efficiency, power added efficiency (PAE) and gain of the EGM amplifier as a function of the output power are shown in Fig. 8. The results match typical class-B PA response configured in balanced PA mode. The maximum output power of the amplifier is higher than 43 dBm (about 20 W). At the peak power, the drain efficiency and PAE of the PA are about 60.5% and 56.7% respectively. The gain of 12.44 dB is achieved at the saturation power.

B. Baseband FPGA Design and Development

In the power amplifier design, the phase and envelope information of the signal are separated and used to drive the PA input and modulate the transistors’ gates respectively. To generate the phase information, a DSP development board from Altera is used [25]. The board includes a Stratix II FPGA to save and analyze the data and two embedded 14-bit, 165-MSPS DAC from the Texas Instruments to generate the I and Q data from the phase of the signal [26].

The second FPGA is used to convert the signal’s envelope to a 1-bit stream signal, using delta-sigma modulation [27], [28]. The generated envelope bit-stream is used to modulate the gates of the EGM PA and driver transistors. The envelope bit-stream speed is very high around 1 GHz and consequently in order to generate such a high speed signal, using another FPGA seems necessary. However, the FPGA used for the envelope in this setup is Altera Stratix II GX which includes very high speed embedded Serializers/De-serializers with the speed clock up to 6.375 GHz [25]. In this case, for example, in order to generate a 1 GHz bit-stream using a 8 × 1 serializer, the envelope signal is needed to be segmented into 8 memories with only clock speed of 125 MHz.
C. Level Shifter, Delay, and IQ Modulator Circuits

The envelope delta-sigma modulated signal should derive the gate biases of the main, auxiliary and digital driver amplifiers. A level shifter circuit is designed and fabricated as an interface circuit between the first FPGA and the power amplifiers to change the voltage levels of the pulses generated from the FPGA to the voltage levels that can switch the main and auxiliary amplifiers of the EGM PA between the on states (VGS = −3.3 V) and off states (VGS = −4.5 V). This circuit can also provide the proper voltage levels (2.7 to 5 volt) for the linear digital driver. The phase information of the signal, programs the second FPGA and then it is up converted to the carrier frequency through a wideband I/Q modulator (ADL5375 from Analog Devices).

The RF modulated phase derives the input of the digital driver and then it is fed to the input of the EGM PA. The delay between the signal’s phase path and the envelope path is calculated and compensated through cables. Therefore, the phase and envelope information of the input signal can be combined properly at the gate levels of the transistors. A bandpass filter is placed at the output of the PA to remove the quantization noise caused by the delta-sigma modulator.

V. MEASUREMENT SETUP AND EXPERIMENTAL RESULTS

Fig. 9 displays the photograph of the proposed transmitter setup. A high Q cavity BPF is also placed at the output of the transmitter setup. The bandpass filter in the EGM transmitter setup contributes in changing the load impedance seen by the amplifiers and also in removing the quantization noise out of the output signal.

A commercial analog cavity bandpass filter, from Anatech Electronics Inc., is used to reconstruct the signal at the output. The filter is centered at the frequency of 2.35 GHz and has the quality factor of about 118. As can be observed in Fig. 10, the...
filter has the 3 dB bandwidth of about 20 MHz. The insertion loss of the filter is about 0.72 dB at the center frequency. Fig. 11 shows the measurement response for the $S_{11}$ phase of the bandpass filter at its input as well as the phase of the reflection coefficient at the combination points of the main and auxiliary amplifiers (at the input of 35 ohm $\lambda/4$ transmission line). It can be observed that the phase at $\pm 500$ MHz away from the center frequency (at 1.85 GHz and 2.85 GHz) is within $\pm 8^\circ$. This phase error is acceptable and one can expect that most of the noise power is reflected back to the power amplifiers.

In order to measure the efficiency performance of the power amplifier for different output power levels, duty cycle pulse test is carried out. In this measurement, pulse trains with variable duty cycles are generated using the first FPGA with the sampling clock rate of $F_s$. Then, the voltage levels of the pulses are adjusted by the level-shifter interface circuits for the gates of the amplifiers (the driver, main, and auxiliary). These pulse trains are used as the envelope signals to switch gates of the transistors on and off. The input signal in this test is an RF carrier at a fixed power level. The efficiency of the power amplifier is measured for each duty cycle value and the results for the sampling frequency of 1 GHz are presented in Fig. 12. In this measurement, the pulse repetition frequency is 100 MHz and the input of the PA is a single tone signal with a fixed power level at the center frequency of 2.35 GHz.

For different duty cycle values, different power levels are expected at the output. For better comparison, the measured drain efficiency of the balanced class-B PA as well as the efficiency of the simulated EGM PA with an ideal high Q bandpass output filter and the theoretical normalized efficiency of EGM PA are also shown in Fig. 12. As can be seen in Fig. 12, the EGM amplifier is more power efficient at back-off power region compared to the balanced class-B amplifier. For instance, the efficiency of the EGM amplifier in this test is about 48% at 6 dB power back off level while the balanced class-B amplifier illustrates the drain efficiency of about 36% at this output power level. At 8 dB back-off power, the drain efficiency of the EGM PA is enhanced about 16% compared with the balanced class-B PA. The deviation of the measurement results from the simulation curve comes from the fact that, that the auxiliary amplifier starts conducting current to the output for gate pulses with duty cycles of
Table I: Summarized performance of the transmitter tested by standard signals with various PAPRs

<table>
<thead>
<tr>
<th>Signal</th>
<th>PAPR [dB]</th>
<th>Gain [dB]</th>
<th>Ave. PAE [%]</th>
<th>Ave. DE [%]</th>
<th>ACLR [dBc]</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDGE 0.27MHz BW</td>
<td>3.1</td>
<td>12.6</td>
<td>55.1</td>
<td>58.3</td>
<td><a href="mailto:-47.8@0.4MHz">-47.8@0.4MHz</a></td>
</tr>
<tr>
<td>LTE up-link 1.4MHz BW</td>
<td>5.0</td>
<td>12.0</td>
<td>50.6</td>
<td>54.0</td>
<td>-37.4@5MHz</td>
</tr>
<tr>
<td>LTE up-link 1.4MHz BW</td>
<td>6.0</td>
<td>11.7</td>
<td>50.4</td>
<td>54.0</td>
<td>-37.4@5MHz</td>
</tr>
<tr>
<td>WiMAX IEEE 802.16e 5MHz BW</td>
<td>7.9</td>
<td>11.0</td>
<td>44.8</td>
<td>48.7</td>
<td>-34.4@10MHz</td>
</tr>
<tr>
<td>WLAN IEEE 802.11a 1.25MHz BW</td>
<td>10.4</td>
<td>9.3</td>
<td>40.8</td>
<td>46.2</td>
<td>-31.4@11MHz</td>
</tr>
<tr>
<td>LTE down-link 5MHz BW</td>
<td>11.0</td>
<td>8.9</td>
<td>40.1</td>
<td>46.1</td>
<td>-38.8@10MHz</td>
</tr>
</tbody>
</table>

Fig. 13: Average drain efficiency, PAE, and gain of the PA tested by modulated signals with various PAPRs versus PAPR in dB.

40%. In this case, the measurement results can be improved by decreasing the average gate bias voltage level of the auxiliary amplifier.

The transmitter setup has also been tested using practical standards’ signals such as EDGE, WiMAX, WLAN and LTE at the center frequency of 2.35 GHz. These signals with different peak-to-average power ratios are utilized to test the performance of the prototype at different power back-off levels. Table I summarizes the performance of the transmitter, tested with different modulated signals with required oversampling ratios, in terms of the measured gain, the average drain efficiency, PAE and ACLR. Fig. 13 also demonstrates the average efficiency and gain of the PA tested by EDGE, LTE, WiMAX and WLAN with 3.1 dB, 5 dB/6 dB, 7.9 dB, 10.4 dB, and 11 dB PAPRs. It can be seen that the average drain efficiency and power added efficiency of the power amplifier is greater than 54% and 50% respectively, when the PAPR of the signal is less than 6 dB. For example, for the 1.4 MHz LTE signal with 6 dB PAPR and oversampled by the ratio of 100, the PA performs with the average drain efficiency of 54.0% and the power added efficiency of 50.4% at the output power of 38.3 dBm.

Using 5 MHz bandwidth WiMAX 802.16e down-link signal with the PAPR of 7.9 dB and the oversampling ratio of 100, the average drain efficiency of 48.7% is achieved at the average output power of 35.8 dBm. The power spectral density of the output signal is shown in Fig. 14. It can be observed from this figure that the ACLR at +10 MHz offset frequency is about –30.72 dBc and at –10 MHz offset frequency is about –34.39 dBc.

For a 5 MHz bandwidth LTE down-link signal with 11 dB PAPR and centered at 2.35 GHz, the power amplifier delivers the average output power of 33.2 dBm. The input signal is oversampled by the ratio of 100. Fig. 15 shows the power spectral density of the output LTE down-link signal along with the mask. For this signal, the PA performs with the average drain efficiency of about 46.1%. The ACLR at the upper 10 MHz offset frequency is measured about –36.85 dBc and at the lower 10 MHz offset frequency is –38.78 dBc. As shown in Fig. 15, the output signal satisfies the LTE signal mask. The performance summary and comparison of our EGM transmitter to other published transmitters based on GaN HEMT transistors with quite the same range of output power is made and the results are summarized in Table II. It can be seen from this table, our design exhibits among highest PAE for WiMAX and LTE downlink signals and good ACLR without linearization. The linearity of the system can be more enhanced by applying digital pre-distortion linearization techniques.

VI. CONCLUSION

In this paper, for the first time a complete transmitter prototype based on GaN HEMT gate modulated power amplifier has
TABLE II

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Efficiency Enhancement Technique</th>
<th>Modulated Signal</th>
<th>PAPR</th>
<th>Signal BW (MHz)</th>
<th>Ave. Pout (dBm)</th>
<th>Ave. PAE (%)</th>
<th>Ave. Eff. (%)</th>
<th>ACLR (dBc)</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>[4]</td>
<td>Hybrid EER</td>
<td>2.65GHz WiMAX</td>
<td>8.2dB</td>
<td>5</td>
<td>42.3</td>
<td>39.5</td>
<td></td>
<td><a href="mailto:-34@7.5MHz">-34@7.5MHz</a></td>
<td>GaN HEMT</td>
</tr>
<tr>
<td>[4]</td>
<td>Envelope Tracking</td>
<td>2.65GHz WiMAX</td>
<td>7.0dB</td>
<td>5</td>
<td>42.0</td>
<td>40.0</td>
<td><a href="mailto:-34@7.5MHz">-34@7.5MHz</a></td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td>[6]</td>
<td>Envelope Tracking</td>
<td>2 GHz LTE Downlink</td>
<td>6.9dB</td>
<td>3</td>
<td>40.18</td>
<td>41.9</td>
<td>-29@4MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-26@4MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td>[6]</td>
<td>EER</td>
<td>2 GHz LTE Downlink</td>
<td>4.8dB</td>
<td>3</td>
<td>40.27</td>
<td>44.2</td>
<td>-26@4MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-28@4MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td>[9]</td>
<td>Doherty</td>
<td>2.14GHz WCDMA</td>
<td>9.8dB</td>
<td>5</td>
<td>36.0</td>
<td>37.8</td>
<td>40.0</td>
<td>-36@4/5MHz</td>
<td>GaN HEMT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-47/54MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td>[10]</td>
<td>Asymmetric Doherty</td>
<td>2.14GHz WCDMA</td>
<td>9.8dB</td>
<td>5</td>
<td>35.2</td>
<td>37.2</td>
<td>-38@4/5MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-45/54MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td>Current Work</td>
<td>EGM</td>
<td>2.35 GHz WiMAX</td>
<td>9.0dB</td>
<td>7</td>
<td>34.2</td>
<td>36.0</td>
<td>40.0</td>
<td>-28@10MHz</td>
<td>GaN HEMT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-45@10MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
<tr>
<td>Current Work</td>
<td>EGM</td>
<td>2.35 GHz WiMAX</td>
<td>7.9dB</td>
<td>5</td>
<td>35.8</td>
<td>44.8</td>
<td>48.7</td>
<td>-34@10MHz</td>
<td>GaN HEMT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-31@10MHz</td>
<td>GaN HEMT</td>
<td></td>
</tr>
</tbody>
</table>

* The ACLR value at the offset frequency is estimated from the reported signal’s spectrum figure. ** DPD denotes the digital pre-distortion.

been proposed for high power applications. Using the advantages of high power gain and high drain-gate breakdown voltages of GaN HEMT devices, a pulsed gate modulated power amplifier has been designed for high power applications. Measurement results using single tone CW signal shows that the PA performs with the drain efficiency of 60.5% and with the PAE of about 56.7% at the maximum output power of 43 dBm. The transmitter has been prototyped and tested first with pulse trains with various duty cycle values. The designed PA demonstrates efficiency enhancement compared with the balanced class-B amplifier (e.g. 12% enhancement in the drain efficiency at the 6 dB OPBO). Practical standards’ signals with various PAPRs have been also used to verify the performance of the complete transmitter prototype and the linearity of the PA. Using a 5 MHz WiMAX signal with 7.9 dB PAPR, the PA performs with the average drain efficiency of 48.7% and the power-added-efficiency of 44.8% at the output power of 35.8 dBm.

REFERENCES


Maryam Jouzdani received the B.Sc. and M.Sc. degrees in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 2007 and 2010, respectively. She is currently pursuing the Ph.D. degree in the Department of Electrical and Computer Engineering, Schulich School of Engineering, University of Calgary, Calgary, AB, Canada. She is now working with the iRadio Lab, University of Calgary, as a Student Research Assistant. Her current research interests are in the areas of microwave active and passive microwave circuit design and power efficient microwave amplification system design.

Mohammad Mojtaba Ebrahimi received the B.Sc. degree in electrical engineering from Amirkabir University of Technology, Tehran, Iran, in 2000, the M.Sc. degree in electrical and computer engineering from Sharif University of Technology, Tehran, Iran, in 2002. He received his Ph.D. degree in electrical and computer engineering, Schulich School of Engineering, University of Calgary, Calgary, AB, Canada, in 2012. In 2012, he joined the iRadio Laboratory, as a postdoctoral fellow and a research assistant. His current research interests include multi-band, multi-branch delta-sigma based transmitter design, switching-mode power amplifiers design, transmitter linearization, and digital signal processing.

Karun Rawat received the B.E degree in electronics and communication engineering from Meerut University, Meerut, India, in 2002. He worked as a Scientist in the Indian Space Research Organization (ISRO) from 2003 to 2007. After that, he joined the iRadio Laboratory of the Schulich School of Engineering, University of Calgary, where he has been working as a Student Research Assistant. He received the Ph.D. degree in the Department of Electrical and Computer Engineering, Schulich School of Engineering, University of Calgary, Calgary, AB, Canada, in 2012. His current research interests are in the areas of microwave active and passive circuit design and advanced transmitter and receiver architecture for software defined radio applications.

Mohamed Helaoui (S’06–M’09) received the M.Sc. degree in communications and information technology from the École Supérieure des Communications de Tunis, Tunis, Tunisia, in 2003 and the Ph.D. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 2008. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, University of Calgary. He has authored or coauthored over 60 publications. He has seven patents pending. His current research interests include digital signal processing, power-efficiency enhancement for wireless transmitters, switching-mode PAs, and advanced transceiver design for SDR and millimeter-wave applications. Dr. Helaoui is a member of the COMMITTAP Chapter, IEEE Southern Alberta Section.

Fadhel M. Ghannouchi (S’84–M’88–SM’93–F’07) is currently an iCORE Professor and Senior Canada Research Chair with the Electrical and Computer Engineering Department, The Schulich School of Engineering, University of Calgary, Calgary, AB, Canada, and Director of the Intelligent RF Radio Laboratory. He has held several invited positions with academic and research institutions in Europe, North America, and Japan. He has provided consulting services to a number of microwave and wireless communications companies. He has authored or coauthored over 500 publications. He holds ten U.S. patents with three pending. His research interests are in the areas of microwave instrumentation and measurements, nonlinear modeling of microwave devices and communications systems, design of power and spectrum efficient microwave amplification systems, and design of intelligent RF transceivers for wireless and satellite communications. Prof. Ghannouchi is a Fellow of the Institution of Engineering and Technology (IET). He is a Distinguished Microwave Lecturer for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).