An Ultra-low Power Predistortion-based FHSS Transmitter

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Abstract—In the new era of personal communications, the energy available for a wireless node is the limiting factor. Furthermore wireless links should be robust even in the harsh indoor environment where fading, attenuation and interferences can be severe. Spread-Spectrum techniques are largely used to have a robust link, while Frequency-Hopping (FH) is the most suitable for low data-rate applications. Unfortunately state-of-the-art FH systems are still too complex and too power hungry to be implemented in a self contained wireless node. The proposed architecture simplifies considerably the hardware requirements for the hopping synthesizer achieving a current consumption of only 900 µA (excluding the output buffer) from a 1.8 V power supply.

I. INTRODUCTION

Many wireless applications in the consumer home nowadays, and in the ambient intelligent home of the future, require a very low data rate (<10 kbps) and a low Quality of Service (QoS). In these cases, standards like Bluetooth and Zigbee provide a much too power-hungry solution, with required current consumption that not easily will allow maintenance-free energy scavenging devices. These devices should be able to transmit and receive reliably data under huge power constraints. Unfortunately, the harsh indoor environment presents, due to fading and strong signal attenuation, a great obstacle to reliable wireless communications when the system is power constrained. Indeed to cope with the non-ideal channel, as well as with multipath fading, and to reduce probability of collision when more wireless nodes transmit at the same time, Spread Spectrum (SS) techniques are commonly employed. In the overcrowded ISM bands, such techniques provide to the wireless nodes the capability to establish a robust link under severe non-ideal conditions.

Among different SS techniques, the most common ones are the Direct Sequence Spread Spectrum (DSSS) and the Frequency Hopping Spread Spectrum (FHSS). The proper choice between DSSS and FHSS depends on the actual environment and application area in which the system will be employed. Due to shorter acquisition time as well as the capability to avoid jammed or deep faded portions of the allowed spectrum, FHSS is the most suitable SS technique for indoor low data-rate applications.

Unfortunately, it generally requires a complex frequency synthesizer in order to generate the hops, which definitely can increase the power consumption well above the allowed limit for a self contained wireless node. Therefore, the design of a minimum complexity hopping frequency synthesizer, which has performances comparable with state-of-the-art hopping frequency synthesizers, is required. This article is organized as follows.

Section II describes the state-of-the-art in FHSS systems. In Section III a new approach towards a minimum complexity hopping synthesizer is proposed, while in Section IV implementation issues and measurement results are given. Finally concluding remarks are given in Section V.

II. FHSS SYSTEMS STATE-OF-THE-ART

The core block of an FHSS system is the frequency synthesizer. Generally, the requirements for an agile and accurate frequency hopping demand a fast settling behavior as well as a high degree of accuracy in the frequency synthesis. Hopping frequency synthesizers are conventionally based on a Phase-Locked Loop (PLL) with a digitally controlled variable divider [1]. Another way to accurately synthesize the frequency bins, is to use a mixed-signal approach. The accuracy and the fast settling behavior are realized through the use of a Direct-Digital Frequency Synthesizer (DDFS) and a Digital-to-Analog Converter (DAC) is used to translate the discrete time periodic waveform from the DDFS in a continuous waveform with specified spectral characteristics [2].

The main sources of power dissipation in a PLL-based frequency synthesizers are the VCO and the frequency divider. In [1] the 900 MHz PLL dissipates 5 mA from a 3 V power supply resulting in a total power consumption of 15 mW, of which 12 mW is dissipated by the VCO.

In a DDFS, a sinewave is synthesized in the digital domain through the use of a simple accumulator and a phase-to-sine amplitude converter. In the simplest case this converter is a Read-Only Memory (ROM). A DAC and a Low-Pass Filter (LPF) are used to convert the sinusoid samples into an analog waveform.

The main operation in a phase accumulator of N-bit length is the N-bit addition. From [3] the energy required for an addition by an Arithmetic and Logical Unit (ALU) can be considered in the range of 250 pJ per addition. If a bandwidth of 9.6 MHz (64 channels spaced by 150 kHz in the 915 MHz ISM band) should be synthesized using the architecture proposed...
in [2], then a 25 MHz reference clock is needed and the power consumption of the phase accumulator can be predicted by the following equation:

$$P_{\text{phase-acc}} = f_{\text{ref-clk}} \times E_{\text{add}}$$  \hspace{1cm} (1)

where $f_{\text{ref-clk}}$ is the reference clock frequency and $E_{\text{add}}$ is the energy per N-bit addition (250 pJ). From (1) the predicted power consumption for the phase accumulator is 6.25 mW. The second block in a DDFS, which generally has significant power consumption, is the ROM. Generally, even if a resolution of few Hertz is needed to keep the spurious level low, practical words longer than 14 bits will lead to a very large ROM even if compression techniques are employed. Considering a truncated 14-bit phase word and a 12-bit wordlength for the amplitude mapping, than the size of the ROM will be approximately 192 kbit. Splitting, for convenience, the ROM in three banks of approximately 64 kbit, then it can be implemented by three $2^4 \times 2^8$ matrices. Defining the storage array as a $2^n = 2^{n-k} \times 2^k$ matrix with $2^n$ memory cells, $2^{n-k}$ rows and $2^k$ columns, then from [4] most of the power consumption in a ROM comes from the pre-charge or the evaluation of the $2^k$ memory cells. Therefore, we can approximate the total power consumption by the following:

$$P_{\text{memcell}} = 3 \times 2^k \left( c_{\text{int}} l_{\text{column}} + 2^{n-k} C_{\text{tr}} \right) V_{\text{dd}} V_{\text{swing}}$$  \hspace{1cm} (2)

where $P_{\text{memcell}}$ is the approximated power consumption of the ROM, the factor 3 takes into account that the total memory has been split in three ROMs of smaller size, $c_{\text{int}}$ is the capacitance of a unit wire length with minimum width, $C_{\text{tr}}$ is the minimum size gate capacitance, $V_{\text{dd}}$ is the power supply voltage and $V_{\text{swing}}$ is the voltage swing of each memory cell. Defining the memory cell as $d_m \times d_m$ square, then the column interconnection length of the memory matrix is $l_{\text{column}} = 2^{n-k} d_m$.

Now, considering as an example the CMOS 0.18 $\mu$m technology, we obtain a predicted power consumption of 5.4 mW. Therefore the power consumption of the DDFS excluding DACs is higher than 10 mW, which is not compatible with the constraints of a self-contained wireless node.

III. PREDISTORTION BASED FHSS FREQUENCY SYNTHESIZER

To reduce the overall power consumption by an order of magnitude, a new architecture is proposed based on the direct synthesis of frequency bins. The schematic block diagram of the proposed architecture is shown in Fig.1.

The incoming data, together with the wanted hopping code, address a particular word cell in the ROM. The ROM has been split into two blocks depending on the modulation bit. In each memory cell the pre-distorted word that will drive the DAC with a defined data bit applied is stored. The DAC then drives directly the varactor array changing the capacitance and therefore the oscillation frequency according to the desired bin and data. The direct frequency synthesis is based on the well known relation between frequency and tank capacitance in a resonator based VCO (LC-VCO for example):

$$f_{\text{osc}} = \frac{1}{2\pi \sqrt{LC}}$$  \hspace{1cm} (3)

where L and C are respectively the total capacitance and inductance of the tank and $f_{\text{osc}}$ is the oscillation frequency. It is possible to change the oscillation frequency of the VCO by varying the capacitance of the tank. This, in practice, is realized by using a varactor diode, which has a capacitance that varies non-linearly with its reverse voltage across it. Therefore, applying the correct voltages to the varactor diodes, it is possible to synthesize all the required frequency bins with minimum hardware complexity (virtually only a VCO).

![Fig. 1. Proposed hopping frequency synthesizer architecture](image)

In an FHSS system the various frequency bins are addressed in a pseudo-random fashion. Pseudo-random codes are generated in the digital domain, while varactor diodes require an analog control voltage. Therefore a DAC is required as interface between the digital world and the analog world. It is important to notice that the DAC employed in a DDFS-based frequency synthesizer works at much higher frequency.

In this new approach the DAC has to be able to give a steady-state voltage at a rate comparable to the hopping rate (kHz range) without any constraint on its dynamic linearity. This will considerably simplify the design of the DAC allowing current consumption as low as 100 $\mu$A [5]. Furthermore, the size of the ROM will be considerably smaller than in a DDFS and equal to $N \times 2 \times 64$ bits, where N is the output word-length that drives the input of the DAC.

To maximize the bandwidth efficiency, so that a crystal-less transmitter can be implemented by using a dedicated digital algorithm at the receiver side [6], and to preserve the code orthogonality, the hopping channels should be arranged in a linear grid. Unfortunately, the chain composed by the DAC, the varactor and the oscillator, introduces some non-linearities:

- Square-root relation between frequency and capacitance
- C-V characteristic of the varactor
- DAC Integral Non-linearity (INL)
To have a grid arranged in a linear fashion, the sum of all these non-linearities should be corrected. Due to the fact that the non-linearities are time invariant, it is possible to apply a pre-distortion technique in the digital domain to correct these non-linearities.

While to preserve the orthogonality between two orthogonal-generated codes the maximum frequency error should not exceed the channel spacing, BER degradation due to phase noise will pose, in practice, an upper bound on the maximum allowed frequency error after predistortion. In the case of 100 kHz spacing between adjacent channels and a maximum 0.5 dB degradation in the SNR at the demodulator input, the maximum residual frequency error is 25 kHz [7]. Furthermore in [7] it is shown that the largest effect on the frequency deviation comes from the varactor non-linearity.

A Simulink™ model of the full TX and RX system has been developed in order to test the new system idea based on pre-distortion. This model has been used to verify the specifications for the DAC in terms of minimum number of bits and maximum INL.

In theory, a 10-bit DAC should produce a maximum residual frequency deviation, due to the quantization error, equal to 15 kHz. In Fig.2 the residual maximum frequency error versus the number of bits in the DAC is plotted. As can be seen, to keep the residual frequency error between TX and RX local oscillators below 25 kHz, which allows no frequency recovery at the receiver through the use of ST-DFT algorithm [8], the minimum number of bits in the DAC should be set to 10. The simulated residual frequency error is around 12 kHz, a value very close to the predicted one.

The varactor has been modeled with a 6th order polynomial, which keeps the maximum frequency error due to the approximation below 3.5 kHz [7]. The DAC INL has been modeled as a second order non-linearity with the maximum INL value placed at the middle code. In Fig. 3 the residual maximum frequency error between TX and RX, for different DAC resolutions as a function of the maximum INL, is shown. Again to keep the residual frequency error below 25 kHz a 10-bit DAC with less than 1.5 LSB INL_{\text{max}} is required.

On the other hand, INL requirements can be traded for DAC resolution giving a degree of freedom in the design.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

The system front-end consists of a resonator based LC-VCO, a divider and an output stage able to deliver -25 dBm power on a 50 Ω load. To minimize oscillator pulling, the VCO operates at 1.8 GHz and divided down to the TX frequency. In Fig. 5 the VCO (550 μA) and the divider are shown. The V_{ff} is the point where the pre-distorted DAC output voltage is applied. The V_{ic} is the coarse control voltage and it is used calibrate the hopping channels inside the ISM band.

The divider is a traveling wave divider. In this design the of ten present external base-resistors of the upper stage are not used and the design is optimized by proper transistor dimensioning to have maximum divider sensitivity at 1.8 GHz and a low power dissipation (200 μA). The output buffer (not shown) is a differential pair (2 mA).

The baseband part has been implemented using discrete components. The microprocessor is the PIC18F627A, which consumes 12 μA at 32 kHz, while the DAC is the AD7392, which draws 100 μA. The measured DAC output is shown in Fig.4. The channel bins are addressed in a sequential way rather than in a pseudorandom fashion. The resulting waveform has a non-linear shape due to predistortion, which compensate for the non-linearities in the transmitter chain. In Fig.6 it is shown the measured spectrum for 64 channels equally spaced by approximately 150 kHz.
Using a software receiver with programmable RF front-end, a complete link has been realized with the implemented TX front-end. For demodulation a short-time DFT algorithm has been implemented as this is most robust to frequency offsets [8]. The measured BER is around 1.1% with an output power of -25 dBm, a distance between TX antenna and RX antenna of 7 meters, in an indoor environment and Non-Line-of-Sight (NLOS) condition. The total measured power consumption is 5.4 mW (including the output buffer).

The IC is realized in SPIRIT, which is produced on SOI wafers followed by a substrate transfer to glass [9]. It is also known as Silicon on Anything (SOA). SPIRIT is a process running in a mass-production foundry, is well-suited for ultra-low power applications due to its high-Q passives, and requires only 15 mask steps. Fig. 7 shows the die-photo of realized TX front-end.

V. Conclusion

In the new era of personal communications, the energy available for a wireless node is the limiting factor. Nevertheless, a robust link is mandatory and can be guaranteed by SS techniques especially in the harsh indoor environment. Among the SS techniques, FHSS, together with BFSK modulation, is the most suitable for low data-rate applications. Unfortunately state-of-the-art FHSS synthesizers are still too power hungry. The proposed innovative FHSS architecture, based on a predistortion algorithm, allows to have at the same time a fast and an accurate synthesis of the frequency bins while requiring an overall power consumption of only 900 µA from a 1.8 V power supply (excluding the output buffer). Using an output buffer able to deliver -25 dBm to a 50Ω matched antenna a complete wireless link has been realized showing a BER of 1.1% with TX and RX antennas placed at 7 meters distance in an indoor environment and a NLOS condition.

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References