An efficient designed prototype technique for OFDM PAPR reduction using FPGA

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SUMMARY

In this paper, a proposed designed technique to reduce OFDM peak-to-average power ratio (PAPR) value is performed. This designed technique contains a new block, which is inserted in the OFDM system. This proposed block is applied to the WiMAX system as an example of the OFDM technology. Afterwards, several MATLAB programs are executed to discuss the behavior and the characteristics of this proposed block. In addition, the effect of its insertion on the original system is studied. Because of this insertion, 0-dB OFDM PAPR value can be achieved. Furthermore, it can be synthesized practically. This proposed system is implemented over a field-programmable gate array (FPGA). The designed circuit is characterized by both its low complexity and its high speed. Moreover, it is a portable circuit. This means that it can be implemented over any FPGA kit regardless of its technology. Copyright © 2012 John Wiley & Sons, Ltd.

Received 23 November 2011; Revised 29 June 2012; Accepted 29 June 2012

KEY WORDS: OFDM; PAPR; FPGA; VHDL

1. INTRODUCTION

OFDM is a method of transmitting data simultaneously over multiple equally spaced carrier frequencies, using Fourier transform processing for modulation and demodulation [1–4].

OFDM offers many well-documented advantages for multicarrier transmission at high data rates, particularly in mobile applications [2]. Therefore, the OFDM system is becoming a key technology extensively deployed in wireless communication systems for broadband access such as wireless local area networks, digital audio and digital video broadcasting, WiFi [5], WiMAX [6], and Long Term Evolution (LTE) [7].

Despite these advantages, there are some drawbacks of OFDM systems such as high dynamics expressed by the peak-to-average power ratio (PAPR) and the subcarriers synchronization [1,4]. The reason for high OFDM signal PAPR is that in the time domain, a multicarrier signal is the sum of many narrowband signals. At some time instances, this sum is large, and at other times, it is small. This means that the peak value of the signal is substantially larger than the average value. This high PAPR is one of the most important implementation challenges that face an OFDM system. That is because it reduces the efficiency and hence increases the cost of the RF power amplifier, which is one of the most expensive components in the radio hardware [4].

In this paper, the PAPR problem will be studied, and briefly some strategies for reducing the PAPR will be offered. Furthermore, a new method is produced to reduce the PAPR value. This new method can achieve 0-dB PAPR value. Afterwards, it is efficiently implemented over field-programmable
gate array (FPGA). The designed circuit is distinguished by both low-complexity and high-speed hardware.

The paper is organized as follows. Section 2 introduces the PAPR problem in an OFDM signal. Section 3 gives an overview of some major existing methods for reducing the PAPR. The proposed method of PAPR reduction is explained in Section 4. The extensive simulation results for the new method and its comparisons with the ordinary OFDM system are made in Section 5. The implementation of the new technique over FPGA is demonstrated in Section 6. Section 7 displays the hardware results for the prototype system. Finally, conclusions are made in Section 8 followed by the relevant references.

2. PAPR

Basically, PAPR is the most popular parameter used to evaluate the dynamic range of the time-domain OFDM signal or signal envelop variation.

The baseband OFDM signal \( s(n) \) as defined in (1) is in fact nothing more than the inverse Fourier transform [3].

\[
s(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k) \exp \left( \frac{j \cdot 2\pi kn}{N} \right)
\]  

(1)

where \( j^2 = -1 \), and \( X(k) \) represents the \( k \)th complex modulated symbol in a block of \( N \) information symbols during the time interval of \([0, T]\).

As OFDM signals are modulated independently in each subcarrier, the combined OFDM signals are likely to have large peak powers at certain instances. The peak power increases as the number of subcarriers increases. The peak power is generally evaluated in terms of PAPR.

Accordingly, the PAPR of the OFDM signal, which is defined as the ratio of the maximum power divided by the average power of the signal, is expressed as

\[
PAPR = 10 \log_{10} \frac{\text{Max} \left[ |s(n)|^2 \right]}{\text{E}[|s(n)|^2]} \text{ (dB)}
\]  

(2)

where \( |s(n)| \) returns the magnitude of \( s(n) \), and \( \text{E}[\cdot] \) denotes the expectation operation [3, 4].

The cumulative distribution function (CDF) of the PAPR of the amplitude \( z \) of an oversampled OFDM signal for \( k \) subcarriers is given in (3) where \( \alpha \) is larger than 1 [3].

\[
P(PAPR \leq z) = (1 - e^{-z})^\alpha
\]  

(3)

3. METHODS OF OFDM PAPR REDUCTION

Many strategies for reducing the PAPR have been accomplished such as clipping [8], coding [9–11], peak windowing [12], and tone reservation [13]. Unfortunately, most of these schemes are unable to achieve a large reduction in the PAPR with a low complexity, low coding overhead, and without performance degradation.

The partial transmit sequence (PTS) method is a well-known method that can reduce the OFDM PAPR value. A major drawback of PTS method is its high computational complexity due to the necessity of a large number of inverse fast Fourier transforms [14–17].

The selective mapping (SLM) scheme is one of the most effective PAPR reduction schemes in OFDM systems. The SLM scheme can achieve several decibels of PAPR reduction and hence significantly improves the transmission power efficiency [18, 19]. One of its major disadvantages is the transmission of side information bits in order to enable the receiver to recover the transmitted data blocks. The reduction of PAPR value in SLM scheme is better than that obtained in the PTS method, but a large number of inverse discrete Fourier transform blocks are required. This results in increased computational and hardware complexity [18].
Dummy sequence insertion (DSI) scheme is another method for PAPR reduction. The drawbacks of the DSI method is that the length of data is increased, which affects the bandwidth. This degrades the transmission efficiency [18, 20].

Additionally, in [21], an efficient technique for the OFDM system using wavelet transform is proposed. It reduces the PAPR value from 8.8 dB for conventional OFDM system to 1.5 dB, whereas in [22], a novel Haar wavelet-based vector binary phase-shift keying–OFDM robust to channel spectral nulls and with reduced cyclic prefix (CP) length and PAPR is proposed. Furthermore in [23], the reduction of dynamic range or PAPR is made by using a proposed root technique. Moreover, in [24], the performance evaluation of OFDM and single-carrier (SC) systems using frequency-domain equalization (FDE) and phase modulation are analyzed. On the basis of the authors’ results, the performance of the continuous phase modulation (CPM) based systems with multipath fading is better than their performance with single path fading by 5 and 12 dB for the OFDM system and the proposed CPM–SC–FDE system, respectively.

4. DESCRIPTION OF THE PROPOSED DESIGNED TECHNIQUE FOR OFDM PAPR REDUCTION

In this section, we will illustrate an efficient designed proposed technique for PAPR reduction. Contrary to traditional techniques, not only PAPR is reduced but also a 0-dB PAPR value with practical solution is obtained. Therefore, the power amplifier of the transmitter can operate at an optimum (saturation) point. Consequently,

- maximizing the average transmit power should be achieved;
- maximizing power amplifier efficiency should be obtained;
- maximizing battery life of the power amplifier should be scored; and
- nonlinear power amplifiers should be used, which are generally more efficient and less expensive than the linear ones.

In the proposed PAPR reduction method, a new block ‘constant amplitude (CA) modulator’ is inserted after the CP insertion block in the OFDM transmitter system, and its reverse block ‘CA de-modulator’ is inserted before the CP removal block in the OFDM receiver system as shown in Figure 1.

The CA modulator can be inserted before the CP insertion block. That is performed to ensure that the channel provides a perfect circular convolution. But in this case, the CP block hardware area will be greatly increased. While inserting the CA modulator after a CP insertion block, one can create an intersymbol interference free channel, without any additional complexity in the CP block.

In order to achieve maximum benefit from the CA modulation, the Hermitian OFDM system should be used. That is because in that system, only real outputs occurred. Therefore, only one CA modulator is used instead of two.
4.1. **CA modulator description**

The structure and the function of CA modulator are displayed in Figure 2. CA modulator consists of three sub-blocks, which are

1. **Inserting Zero sub-block**: Its function is to insert a leading zero sample to each OFDM sample. Accordingly, the first sample of each OFDM symbol is known, and it is equal to zero.
2. **Inserting samples sub-block**: Its function is to insert extra samples between each two adjacent samples. These extra samples are gradually increased or decreased according to the primitive samples. Hence, the sampling rate is increased after this sub-block by the number of inserted samples. On the one hand, the more samples are inserted, the more accurate results are obtained. On the other hand, the more hardware complexity is suffered.
3. **Comparing samples sub-block**: Its function is to compare each two adjacent samples $s(i)$ and $s(i-1)$ as follows:
   
   (a) If $s(i) > s(i-1)$, the output will be $+0.5$.
   (b) If $s(i) < s(i-1)$, the output will be $-0.5$.
   (c) If $s(i) = s(i-1)$, the output will be 0.

   Therefore, the output of this block always has a constant amplitude with no peaks. That is because it has only $\pm 0.5$ values, whereas the zero value of the output very rarely occurs because of the phenomenon of OFDM signal.

4.2. **CA de-modulator description**

At the receiver, the inverse operations are carried out in the CA de-modulator as shown in Figure 2. The CA de-modulator consists of three sub-blocks, which are

1. **Samples generation sub-block**: Its function is to regenerate the OFDM signal with the residual samples from the received signal. That is performed by setting the first sample to zero (as we are sure of that by inserting zero sub-block). Then the proceeding samples are computed one by one as follows:
   
   (a) If the received sample > zero, the output sample value = the previous one + the step size.
   (b) If the received sample < zero, the output sample value = the previous one − the step size.
   (c) If the received sample = zero, the output sample value = the previous one.

   The step size is selected to be the reciprocal of (the number of extra inserted samples in the transmitter + 1).

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**Figure 2. CA modulator and CA de-modulator structures.**
2. Removing residual samples sub-block: Its function is to remove the extra samples inserted by ‘inserting samples sub-block’. Therefore, the output of this block is less sampling rate than its input (i.e., the same sampling rate of the original OFDM input signal to the CA modulator).
3. Removing leading zero sub-block: Its function is to remove the leading zero that is inserted in the transmitter in order to know the value of the first sample. Then correct estimation of the samples values at the receiver can be carried out.

5. SIMULATION RESULTS

In this section, the proposed new block is studied through MATLAB simulation. To gain an appreciation for the time and frequency domain interpretations and the PAPR of the modified OFDM, the WiMAX system can be used as an example. The WiMAX and the CA modulation block parameters used for this simulation are illustrated in Table I.

5.1. The effect of the CA modulator on original system

The overall simulation system is shown in Figure 3. The CA modulator block is inserted twice, one for real output and the other for imaginary output. After running the simulation, both the ordinary and modified OFDM systems give zero bit error rate, which means that the bits are correctly recovered without any errors.

To discuss the effect of our CA modulation, both time and frequency domains of the ordinary system and the modified one are examined.

Table I. Simulation area parameters.

<table>
<thead>
<tr>
<th>WiMAX parameters</th>
<th>Channel BW</th>
<th>20 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP length</td>
<td>1/16</td>
<td></td>
</tr>
<tr>
<td>Oversampling ratio</td>
<td>57/50</td>
<td></td>
</tr>
<tr>
<td>FFT length (NFFT)</td>
<td>256</td>
<td></td>
</tr>
<tr>
<td>Data length (Nused)</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>Modulation scheme</td>
<td>QPSK</td>
<td></td>
</tr>
<tr>
<td>Coding rate</td>
<td>1/2</td>
<td></td>
</tr>
<tr>
<td>CA modulation parameters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Excess samples between each two adjacent samples</td>
<td>63</td>
<td></td>
</tr>
<tr>
<td>Step size</td>
<td>1/64</td>
<td></td>
</tr>
<tr>
<td>Output values</td>
<td>0 ± 0.5</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3. The simulation system of the modified model.
From Figure 3, the real part of the original received signal is tested from the point ‘A1’, whereas for the modified system, the real part of the received signal is taken at the point ‘A3’. By the same way, the imaginary part testing points are taken at the points ‘A2’ and ‘A4’ for original and modified system, respectively.

Figures 4 and 5, display a pattern of the time domain of the real and imaginary parts of the OFDM received signal for the two systems, respectively. It is noticed that the OFDM signal is nearly not affected by our CA modulation. Thus, our CA modulation can almost perfectly track the original OFDM signal. The reason for that is the presence of the ‘inserting samples sub-block’. Additionally, the OFDM signal recovery is directly affected by the number of extra inserted samples. Therefore, the CA modulator produces very few errors, which will be removed from the rest of the system by quadrature phase-shift keying (QPSK) de-modulator.

Figure 6 produces the frequency domain of the real part of the OFDM received signal for both systems. According to the nearly perfect tracking of OFDM signal, the frequency domain is not affected by the proposed CA modulation.
5.2. The CA modulator characteristics discussion

From previous results, the original signal is not distorted by the presence of the CA modulator. Now, the characteristics of the CA modulator are illustrated. Both time and frequency domains of the modified real output OFDM signal are shown in Figures 7 and 8, respectively.
It is noticeable that constant amplitude of the output OFDM signal is achieved. On the contrary, the ordinary system has unpredictable peaks. Therefore, the PAPR of the modified system should be reduced.

On the other hand, it is observed that the growth of the required signal bandwidth will be needed. This is because of the extra samples inserted in the CA modulator. Therefore, the bandwidth of the measured spectrum is increased without changing its frequency resolution by a factor of the number of the inserted extra samples. Clearly, this is considered the major drawback of our block.

The main advantage of the proposed CA modulator is the 0-dB PAPR achievable value. Figure 9 describes the complementary CDF for both ordinary and modified systems. It is clear that the ordinary WiMAX system has PAPR values in the range 8.5–14.5 dB, whereas the proposed modified system has 0-dB PAPR value. That is because of the constant amplitude achieved by the proposed block ‘CA modulator’. This means that there are no peaks in the transmitted signal as shown in Figure 7.

5.3. CA modulation advantages

It is worth clarifying that our CA modulation is not a delta modulation. That is because the delta modulation has only two cases of comparison and not three as in the CA modulator. In addition, there are no insertion for any zero or residual samples in the delta modulation. Also, there is no low path filter in the CA de-modulator as in the delta de-modulator. For another side, the CA modulation has several advantages listed as follows:

- It is a simple method compared with many other traditional techniques for PAPR reduction such as PTS, SLM, and DSI.
- It is a very efficient method as it can achieve a 0-dB PAPR value as we will see in Section 7. That is because the output of the CA modulator has constant amplitude.
- It is an applicable method contrary to some other previous methods such as companding.
- The output of the CA modulator has only ±0.5 values in addition to a zero value, which rarely occurs. Therefore, the D/A converter will be very simple, and hence, the cost and complexity will be reduced.
- The recovered signal is the same as the input signal. That is due to the inserting zero and the inserting samples sub-blocks, as the leading zero helps the de-modulator to accurately track and recover the original signal. On the other hand, the more extra samples inserted by ‘inserting samples sub-block’, the more accurate results are achieved.
5.4. CA modulation disadvantages

One drawback of our CA modulation is that the excess samples are not part of our data. Then the efficiency of the transmission throughput is reduced. Also, increasing the sampling rate for a fixed duration is to increase the bandwidth of the measured spectrum without changing its frequency resolution. One other disadvantage is the trade-off between the accurate results and the number of excess samples. Additionally, the OFDM system has penalty of the extra block ‘CA modulator’ in order to reduce the PAPR value.

6. IMPLEMENTATION OF THE PROPOSED TECHNIQUE OVER FPGA

In this section, the proposed CA modulator is implemented and tested as a real hardware over FPGA. Firstly, a brief introduction for FPGA is introduced. Then the prototype hardware parameters description of the modified OFDM system with CA modulator is illustrated.

6.1. FPGA brief background

FPGAs are digital integrated circuits (ICs) that contain programmable blocks of logic along with configurable interconnects between these blocks. Design engineers can program such devices to perform a tremendous variety of tasks. VHDL stands for VHSIC (very high-speed IC) Hardware Description Language, which is commonly used as a design entry language for FPGA and ASIC devices. There are many applications of FPGAs, which include digital signal processing, software-defined radio, aerospace and defense systems, speech recognition, computer hardware emulation, and a growing range of other areas [25–27].

6.2. The modified OFDM system with CA modulator/de-modulator hardware parameters

The eight-point OFDM system can be used as an example to be implemented over FPGA. Therefore, the modified prototype OFDM system is shown in Figure 1, taking an eight-point I/FFT size, assuming all symbols are data, and supposing CP are two samples. Also, the number of extra inserted samples is taken to be seven samples. Thus, the step size of the CA de-modulator is \( \frac{1}{8} \).

In order to make an efficient hardware, a Hermitian OFDM is used. Therefore, only real outputs will appear. Then only one CA modulator is needed. Moreover, the D/A and the A/D are not implemented in our hardware, as we connect the output of the CA modulator directly with the input of the CA de-modulator. Additionally, a fixed point representation is used instead of floating point to present the samples values. Therefore, the hardware area for the adder/subtraction/multiplier circuits and the I/FFT circuit will be greatly reduced than in [28, 29], respectively.

The proposed CA modulator/de-modulator circuit interface structure is shown in Figure 10, and the associated pin functionality is described in Table II.

Figure 10. CA modulator/de-modulator core interface.
### Table II. \(\text{I/O pins functionality description.}\)

<table>
<thead>
<tr>
<th>Pin name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk1</td>
<td>Input</td>
<td>Slow master clock for leading zero sub-block (active rising high)</td>
</tr>
<tr>
<td>clk2</td>
<td>Input</td>
<td>Fast master clock for the rest sub-blocks (active rising high and equals to (8\times \text{clk1}))</td>
</tr>
<tr>
<td>rst</td>
<td>Input</td>
<td>Master asynchronous reset (active high)</td>
</tr>
<tr>
<td>en</td>
<td>Input</td>
<td>It is asserted high for each incoming OFDM symbol to begin processing</td>
</tr>
<tr>
<td>sin(9:0)</td>
<td>Input</td>
<td>The input OFDM samples. It is 10 bits fixed point format</td>
</tr>
<tr>
<td>sout(1:0)</td>
<td>Output</td>
<td>The output OFDM samples of the CA modulator. It is 2 bits fixed point format</td>
</tr>
<tr>
<td>en_o</td>
<td>Output</td>
<td>It is asserted high for each outcoming OFDM symbol</td>
</tr>
<tr>
<td>en_s</td>
<td>Output</td>
<td>It is asserted high for each original sample (without the excess samples)</td>
</tr>
</tbody>
</table>

### Table III. The synthesis, and place and route summary reports.

<table>
<thead>
<tr>
<th></th>
<th>CA modulator</th>
<th>CA de-modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Synthesis report</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of slices</td>
<td>92 out of 13 696</td>
<td>10 out of 13 696</td>
</tr>
<tr>
<td>Number of slice flip flops</td>
<td>99 out of 27 392</td>
<td>16 out of 27 392</td>
</tr>
<tr>
<td>Number of 4 input LUTs</td>
<td>166 out of 27 392</td>
<td>17 out of 27 392</td>
</tr>
<tr>
<td>Number of IOs</td>
<td>18 out of 556</td>
<td>18 out of 556</td>
</tr>
<tr>
<td>Number of GCLKs</td>
<td>2 out of 16</td>
<td>1 out of 16</td>
</tr>
<tr>
<td><strong>Place and route report</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of slices</td>
<td>99 out of 13 696</td>
<td>16 out of 13 696</td>
</tr>
<tr>
<td>Number of IOs</td>
<td>18 out of 556</td>
<td>18 out of 556</td>
</tr>
<tr>
<td>Number of BUFGMUXs</td>
<td>2 out of 16</td>
<td>1 out of 16</td>
</tr>
</tbody>
</table>

7. HARDWARE RESULTS

In this section, the hardware area and timing constraints are reported. In addition, the timing output of the circuit is obtained for both original and modified systems.

This system is designed using VHDL. The VHDL code is achieved following the recommendations of [27, 30, 31]. No pre-designed component available from the libraries of any EDA vendor is used. Therefore, this design can be applied to any synthesis tools and enables the portability among different technologies. Moreover, the system is synthesized using an ISE synthesis tool. The behavior and timing simulations are carried out using Modelsim EDA tool (which is introduced by Mentor Graphics FPGA Advantage 7.0 PS) [32, 33].

#### 7.1. The hardware area reports

The synthesis, and place and route summary reports of the ISE tool for Xilinx, Virtex2p family, xc2vp30 device, are displayed in Table III. It can be declared that the hardware area is consumed by CA modulator/de-modulator. Therefore, our proposed block is simple and can be efficiently applicable.

#### 7.2. The hardware speed report

From the ISE synthesis tool, the maximum clock frequency (in order to not obtain distorted results), which can be applied to the CA modulator circuit, is 272.327 MHz, whereas the maximum clock frequency for the CA de-modulator circuit is 414.800 MHz. Indeed, this is a very-high-speed circuit for both modulator and de-modulator. Therefore, our proposed circuit not only has
7.3. The timing simulation

To test the correctness of our implemented modified system, a random input is inserted to the modified OFDM system transmitter. Then the output from the receiver is checked. The system should give back the same value of the input, and this actually occurred as shown in Figure 11. Therefore, our modified system works effectively. It is worth clarifying that the overall execution time for the modified OFDM system (from the input of the transmitter till the appeared output at the receiver) is 37 clocks cycles (i.e., 7.4 μs with a 5-MHz operating frequency). As a result, our modified OFDM system is considered a very-time-efficient system.

Additionally, a MATLAB program is used to verify the authenticity of the proposed system. The implemented circuit original OFDM signal output is compared with the recovered modified one as displayed in Figure 12. It is cleared that few errors are produced by the proposed circuit. That is because of the hardware quantization errors, as fixed points numbers are used to demonstrate the samples values. Therefore, the direct relationship between the fraction resolution and the output accuracy is presented.

8. CONCLUSIONS

A proposed designed technique has been deeply explained for OFDM PAPR reduction. A proposed designed block named by CA modulator has been inserted in the original OFDM system. This proposed block has converted the original OFDM signal to a constant amplitude square wave with no peaks. Therefore, a 0-dB PAPR value has been achieved when simulated in a WiMAX environment.
Extensive MATLAB simulation programs have been performed to discuss the characteristics and the effects of the proposed designed block. It has been shown that the proposed designed inserted block has had several advantages such as its simplicity and reliability. Additionally, it could be synthesized practically as a prototype circuit. Moreover, the 0-dB PAPR value could be obtained. The main drawback of the proposed system has been the need for the growth of the bandwidth. Furthermore, the proposed designed technique has been implemented as a real-time prototype circuit over FPGA using the VHDL language. The designed system has been efficiently synthesized to be portable, of low complexity, and a high-speed system. Moreover, the designed circuit has been tested to verify its function.

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N. El-Fishawy received her PhD degree in Mobile Communications from the Faculty of Electronic Engineering, Menoufia University, Menouf, Egypt, in collaboration with Southampton University in 1991. Now, she is the head of Computer Science and Engineering Department, Faculty of Electronic Engineering. Her research interest includes computer communication networks with emphasis on protocol design, traffic modeling and performance evaluation of broadband networks, and multiple access control protocols for wireless communications systems and networks. Now, she directed her research interests to the developments of security over wireless communications networks (mobile communications, WLAN, and Bluetooth), VOIP, and encryption algorithms. She has served as a reviewer for many national and international journals and conferences. Also, she participated in many technical program committees of major international conferences in wireless communications.

S. El-Rabiae (senior member, IEEE’1992-MI EE-Chartered Electrical Engineer) was born in Sires Elian (Menoufia), Egypt in 1953. He received his PhD degree in Microwave Device Engineering from the Queen’s University of Belfast, 1986. He was a postdoctoral fellow at Queen’s University (Department of Electronic Eng.) up to February 1989. In his doctoral research, he constructed a CAD package used in nonlinear circuit simulations based on the harmonic balance techniques. Since then, he has been involved in different research areas including CAD of nonlinear microwave circuits, nanotechnology, digital communication systems, and digital image processing. He was invited in 1992 as a research fellow in the North Arizona University (College of Engineering and Technology) and in 1994 as a visiting professor in Ecole Polytechnique de Montreal (Quebec), Canada. He has authored and co-authored more than 120 papers and technical reports and 15 books. In 1993, he was awarded the Egyptian Academic Scientific Research Award (Salah Amer Award of Electronics) and in 1995, he received the award of the Best Researcher on (CAD) from Menoufia University. He has shared in translating the first part of the Arabic encyclopedia. He was the head of the Electronic and Communication Engineering Department, Faculty of Electronic Engineering, Menoufia University and then the vice dean of Postgraduate Studies and Research in the same faculty. Now, he is a professor of the Electronic and Communication Engineering, Faculty of Electronic Engineering, Menoufia University.

M. Shokair works as a lecturer in the Department of Electronics and Electrical Communications and the Faculty of Electronic Engineering. Her research areas of interest include mobile communication systems, OFDM systems, single carrier FDMA (SCFDMA) systems, interference cancellation, and cognitive radio.