Complements on Phase Noise Analysis and Design of CMOS Ring Oscillators

Timothy Cronin1,2, Domenico Pepe1, and Domenico Zito1,2
1Tyndall National Institute, Lee Maltings, Dyke Parade, Cork, Ireland
2Dept. of Electrical and Electronic Engineering, University College Cork, College Road, Cork, Ireland
Email: domenico.zito@tyndall.ie

Abstract—This paper reports two complements on phase noise analysis and design of CMOS ring oscillators. In detail, it proposes an extension to current analytical methods for predicting flicker noise contribution to phase noise in differential CMOS ring oscillators. The results of the proposed analysis are compared with the existing methods and simulation results by SpectreRF for two differential topologies. The comparative analyses confirm that the proposed method leads to an improvement of the prediction accuracy in spite of the small increase of complexity since it only requires device dimensions in addition to the data required by existing methods. The proposed method may also be used to indicate a minimum achievable close-in phase noise in a process node. Moreover, a design approach for low phase noise inverter-based ring oscillator is proposed and tested by means of simulation. The limitations of the proposed method can be observed from this case study.

I. INTRODUCTION

Recent efforts in radio frequency integrated circuit (RFIC) design have been geared toward implementing front-end operating at high frequencies, in processes optimized for digital circuitry [1]. This increased integration reduces fabrication costs of the building blocks and, hence, the overall system. Ring oscillators can be implemented using only transistors, and, more importantly, without spiral inductors characterized by a large area occupancy. This makes ring oscillators very attractive for integration with existing functional blocks on silicon. The main drawback of ring oscillators is the poor phase noise performance. In spite of this, the attractive fabrication costs of CMOS technology are likely to drive innovation in the mass-market implementation of wireless chipsets for short range, and possibly cellular, communications in more and more advanced technology nodes. It is the goal of this paper to accelerate progress by improving the understanding of oscillator phase noise performance. In the last decade accurate hand analyses of phase noise in ring oscillators requiring minimal computational effort have been proposed in [2], [3]. Since then, refinements to [2] have been proposed in [4]. These require additional computational efforts in time domain waveform analysis and deal with white noise contributions, whose resultant effects are predominant for large frequency offsets from the carrier, only. Another work, [5], has established a lower bound on attainable phase noise in switched-based oscillators. However it is also limited to the effects of white noise only, leaving uncovered the predictive analysis of minimum achievable phase noise for

This work is supported by Science Foundation Ireland (SFI).

Moreover, a design methodology for low phase noise ring oscillators was proposed in [3]. This is based on the idea that if the rms impulse sensitivity function (ISF) of a oscillator is minimized, its phase noise will also be minimized. The ISF can be reduced by minimizing the portion of the period in which the oscillator changes state, i.e. the switching time of the delay stages. This could be implemented by means of a large number (long ring) of fast delay stages. This seems to have remained unexplored in the literature and is reported herein.

The paper is organized as follows. Section II reports the existing phase noise estimation methods for differential rings, as well as the proposed extension to flicker noise contributions for an improved accuracy. Section III encompasses the rationale for a low phase noise long ring oscillator design with minimal rms ISF, and the potential issues with such a design approach. Section IV includes the results of circuit simulations in Cadence design environment in order to verify the validity of analysis. Finally, in Section V, the results are discussed, and in Section VI, the conclusions are drawn.

II. PHASE NOISE ANALYSIS

A. Existing Methods

Phase noise \( L(f) \), in an electrical oscillator arises from intrinsic electrical noise sources altering the bias conditions of the circuit and, hence, its tuning. This manifests itself as a distribution of the oscillation signal power over a spectrum in the frequency domain and as random accelerations and decelerations of phase in time. \( f \) represents an offset from the nominal oscillation frequency \( f_0 \). In order to calculate phase noise, therefore, the variation in phase must be calculated. A method for estimating phase noise in resistively loaded differential ring oscillators is proposed in [2]. This accounts for noise in the channel of \( M_h \), which forms multiple current mirrors with the tail transistors \( M_t \), in Fig.1. Flicker noise propagated in this way into the ring dominates the phase noise performance because it is coupled to all the gates of \( M_h \) and, hence, it is correlated over all stages. In [2], phase noise