Characterization of high-voltage IGBT module degradations under PWM power cycling test at high ambient temperature

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\begin{abstract}
The success of the high temperature power electronic applications depends on the power device reliability. The increasing thermal demands, like in hybrid electric cars, require power devices operating at junction temperatures above their common level of 125°C. The thermal cycles generated in standard modules in such conditions induce several failure mechanisms in their package and chips. This article presents ageing tests of an EconoPIM IGBT module submitted to PWM power cycling at high ambient temperature. Several electrical and thermal parameters are monitored to detect failure onsets in the module components. Static and dynamic measurements are periodically made to reveal possible module characteristic drifts, and to better understand the effects of this kind of cycling test on the module static and switching behaviors. The follow-up of the dynamic parameter evolution represents the originality of this study.
\end{abstract}

1. Introduction

In many applications, particularly in military, industrial and chemical electronics, there is an increasing interest for power devices operating at high temperatures. These devices have then to fulfill high reliability requirements under harsh environmental conditions. The chip self-heating combined with the cooling conditions induces strong thermal stress in the devices, which can progressively conduct them to fatal failures.

Many previous works, based on test specifications established in RAPSDRA and LESIT projects \cite{1,2}, have led to a good knowledge of the failure physics caused by power cycling on power devices particularly in railway traction applications \cite{3–7}. The standard packaging and interconnection technologies can not withstand intensive thermal cycles due to the mismatched thermal expansion coefficients between the assembly components. The main weak points are the bond wire area and the solder layers in the chip/substrate and the substrate/base plate interfaces \cite{3–7}. The thermal stress can also lead to cracks in the substrate, reconstruction of the chip metallization, die fracture and degradation of the silicone oxide layer \cite{6,7}. Manufacturers have then developed some packaging concepts and interconnection improvements \cite{8–10}.

The majority of power cycling tests performed on IGBT modules use constant DC load current \cite{11}. Other current forms are poorly investigated. To approach the real operating conditions, this article introduces Pulse Width Modulation (PWM) power cycling test carried out on an EconoPIM IGBT module at 80°C ambient temperature and at junction temperature swings AT, of 70 K. The switching and the conduction losses are combined to speed up the ageing phenomenon and thus to activate the assembly failure modes. The aim is to understand the failure modes induced by this kind of cycling test, to characterize the module static behavior and to show if the cycling diminishes the module dynamic performances. The follow-up of the switching parameter evolution during the cycling test completes the obtained results in the previous studies.

2. Power cycling test methodology

The test bench, developed in our laboratory, allows power cycling tests with constant DC or PWM load current (with variable duty cycle) during the power injection phases, and with the possibility of heating the module base plate to a desired temperature. It is monitored by a control unit which commands the DUT conduction.

The tested device is an EconoPIM 1200 V–15 A IGBT module (see Fig. 1) from Eupec. Among the important features of EconoPIM technology, all internal contacts between chip, frame-terminals and top copper layer are realized by thick aluminum bond wires and the load current is divided on several parallel terminals to optimize the power distribution on the module printed circuit board \cite{12}.

The ageing test is achieved under low voltage, by cyclic PWM power injection with 10 s power on (t\textsubscript{on}) and 20 s power off (t\textsubscript{off})
Research projects and experimental works, conducted since 1994, have identified three major failure modes associated to failure criteria defined as follows [1–3]:

- Forward voltage drop $V_{CE(sat)}$ increasing of 5% with respect to initial value due to sudden lift-off or heel cracking in the bond wires.
- Junction to heat sink thermal resistance $R_{th(j-h)}$ increasing of 20% with respect to initial value due to delamination or crack initiation in the solder layers.
- Leakage current $I_{CES}$ increasing due to degradation of the siliccone oxide layer.

During the test, these indicators are measured or calculated in order to diagnose failure imminence.

4. Ageing test results in the IGBT assembly

Testing of the considered IGBT module was completed after 170 kcycles and the obtained results are summarized in this section. Fig. 3 shows exceeding of the specific limit of both monitored indicators, $R_{th(j-h)}$ and $V_{CE(sat)}$, respectively at 155 and 165 kcycles. The cycling test was stopped because of harmful junction temperatures reached at the last cycles (see Fig. 4) then a failure analysis was conducted.

Note that in order to avoid abrupt voltage drops after test-restarts, as it appears on the $V_{CE(sat)}$ graphic at 63 kcycles, the static measurements were done after removing the DUT from its heat sink only at this specific level. The later static and dynamic measurements were done without disassembling the device from heat sink.

The $V_{CE(sat)}$ drop at 63 kcycles is often observed in power cycling tests on IGBT with positive temperature coefficient and is a consequence of a decreasing of the thermal resistance $R_{th(j-h)}$. This is due to the thermal extension of the substrate which enhances the distribution process of the thermal grease and improves the thermal conductivity of the assemblies [13,14]. For this reason, it can be seen a correlative decrease of the maximum junction temperature $T_{jmax}$ (see Fig. 4). This behavior does not appear in the graphics at the first cycles because of long calibration tests that were done before the start of the cycling. The progressive decreases, until 63 kcycles, of $V_{CE(sat)}$ and $T_{jmax}$ are related to the spreading out of the thermal grease.

### 3. Failure criteria

<table>
<thead>
<tr>
<th>Number of cycles x 10^4</th>
<th>$V_{CE(sat)}$ (mV)</th>
<th>Specification limit</th>
<th>$V_{CE(sat)}$ increase 5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>4000</td>
<td>4100</td>
<td>4500</td>
</tr>
<tr>
<td>5</td>
<td>4200</td>
<td>4300</td>
<td>4600</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Number of cycles x 10^4</th>
<th>$R_{th(j-h)}$ (K/W)</th>
<th>Specification limit</th>
<th>$R_{th(j-h)}$ increase 20%</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.9</td>
<td>1.1</td>
<td>1.3</td>
</tr>
<tr>
<td>5</td>
<td>1.1</td>
<td>1.3</td>
<td>1.5</td>
</tr>
</tbody>
</table>
A scanning electron microscopy (SEM) analysis was performed. The results do not reveal important failures. The main effect on the bond wire area that was observed is the degradation of a single bond wire at an intermediate connection on a top copper layer (see Fig. 5). It is a deterioration of the upper bond wire heel, which is well shown by the magnified part of Fig. 5. This might explain the sudden leap of $V_{CE(sat)}$ at 128 kcycles, which maintains a progressive increase of this voltage until the exceeding of the specific limit at 165 kcycles, where bond wire lift-off should happen. This latter effect might be observed through a more thorough SEM analysis because the active thermal stress is harsher in the bond wire area than on the copper layers.

The other results concern the degradations of the emitter and gate metallization, as shown respectively in Figs. 6 and 7. It can be seen a beginning of aluminum grains dislocation on their surfaces, which can weaken the connections and reduce the electric conductivity [7].

The evolution of the thermal resistance $R_{th(j-h)}$, that is shown in the lower part of Fig. 3, proves failure occurrences in the solder layers. Unfortunately, no scanning acoustic microscopy (SAM) analysis could have been done due to lack of appropriate instruments. Such an analysis would surely show delamination process in the solder layers. This is suggested by the exponential increase of the junction temperature $T_{jmax}$ (see Fig. 4) after the exceeding of the $R_{th(j-h)}$ increasing limit. This attests of a bad dissipation of the generated heat in the chip which leads to increase the thermal resistance of the device and thus enlarges the thermal stress inside the package. Note that the employed fan allows efficient cooling of the device even when $T_{jmax}$ reaches high values, such that the $T_{jmin}$ values remain almost constant, around 90 °C.

5. Influence of PWM active cycling on the IGBT static and dynamic parameters

In this section, we present the results of the static and dynamic measurements. No influences were noted neither on the threshold voltage $V_{GE(th)}$ (see Fig. 8) nor on the breakdown voltage $V_{BR(CES)}$ (not shown here). This contradicts a slight increase of $V_{GE(th)}$ of about 300 mV obtained in previous power cycling test using constant DC load current [6].

The next graphic (see Fig. 9) exhibits a quite constant evolution of the gate–emitter leakage current $I_{GES}$ although a slight decrease is observed at the beginning. This proves that the gate oxide layer is not affected under our test conditions. In contrast, gate leakage failures were observed in previous works [6,11].

Fig. 10 shows that the cycling has caused a slight decrease of the collector leakage current $I_{CES}$ which might be related to a small increase of the collector–emitter resistance, due to bond wire degradation.

Figs. 11, 12 and Figs. 13, 14 highlight respectively early beginning of switching-on and switching-off waveforms under cycling as compared to the dynamic performances before the cycling test. These waveforms were obtained under the same conditions.

It can be seen on these figures that stabilized dynamics are attained beginning from 138 kcycles to the end of the test. The time...
shift is more important for the turn-off mode (see Figs. 11 and 13), where the earlier response might be related to faster discharge of the IGBT parasitic capacitances. The corresponding Miller plateau width is smaller than in the turn-on mode, as it appears in gate voltage waveforms (see Figs. 12 and 14).

The appearance of a tail-current observed in all the current $I_{C-Off}$ waveforms is unexpected and was never mentioned in previous studies [11]. It seems that the PWM cycling affects the base region intrinsic properties and diminishes the device blocking capability.

Further results including the turn-on and turn-off delays ($t_{\text{d-on}}, t_{\text{d-off}}$), the rise and fall times ($t_r, t_f$) are presented in Figs. 15 and 16. The following facts can be noted:

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**Fig. 9.** Evolution of the gate leakage current under cycling.

**Fig. 10.** Evolution of the $I_{CES}$ leakage current under cycling.

**Fig. 11.** Comparison of $I_C$ and $V_{CE}$ switching-on waveforms.

**Fig. 12.** Comparison of $V_{CE}$ switching-on waveforms.

**Fig. 13.** Comparison of $I_C$ and $V_{CE}$ switching-off waveforms.

**Fig. 14.** Comparison of $V_{CE}$ switching-off waveforms.

**Fig. 15.** Evolution of the turn-on $t_{\text{d-on}}$ and the turn-off $t_{\text{d-off}}$ delays.
– A significant decrease of $I_{d-off}$ which is related to the decrease of the Miller plateau duration.
– A significant increase of the fall time $t_f$ which is related to the earlier turn-off mode.
– The variations of $I_{d-on}$ and $t_r$ are smaller due to the less earlier turn-on mode.

We can also note that the previous variations do not alter the switching speed of the device. In fact, the turn-on delay plus the rise time and the turn-off delay plus the fall time remain almost constant before and after cycling.

6. Conclusion

The accelerated power cycling test, presented in this paper, is based on PWM power injection mode on a high-voltage IGBT module at high ambient temperature and high junction temperature swings. This operating mode is more realistic than that adopted in usual DC power cycling tests (using constant load current). Firstly, the aim was to show if the thermo-mechanical stress leads to more failure modes since the switching and the conduction losses are combined to speed up the ageing phenomenon and secondly to know the effects of this kind of cycling on the module dynamic performances.

Concerning the induced failures, the follow-up of the both monitored indicators, $R_{D_{(on)}}$ and $V_{CE(sat)}$, shows exceeding of their specific limits respectively at 155 and 165 kcycles but the SEM analysis do not reveal important failure modes in the chip area. The observed degradations concern a deterioration of a bond wire mounted on copper layer, a beginning of aluminum grains dislocation on the surfaces of the gate and emitter metallization. The most important failure concerns the delamination in the solders layers even if a SAM analysis was not performed. This failure is obvious because of the exponential increase of the junction temperature, due to very bad heat dissipation in the device, at the last cycles. We think that all the degradations must be verified through more thorough SEM and SAM analyses because the active thermal stress is important in the assembly. Usually, DC power cycling tests exhibit drastic failures of the bond wires on the ship area, the emitter metallization, the solder attaches [3–7].

The other interesting results concern the dynamic performances of the device. The accelerated ageing test led to earlier turn-on and turn-off modes, with a significant reduction of the turn-off delay, an increase of the fall time, and a less significant variation of the turn-on delay and the rise time. Note that these variations do not really alter the switching speed of the device before and after cycling. An unexpected result is the appearance of a tail-current after cycling which might affect the blocking capability of the device. This later effect was not obtained with DC power cycling test [11].

Same PWM power cycling test should be conducted repeatedly on other devices in order to confirm the results presented in this paper. The test conditions (power on and power off durations, the heat sink regulated temperature, the junction temperature swing) may be changed to evaluate the effects of the induced thermo-mechanical stress on the module assembly and on its static and dynamic performances.

Acknowledgement

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References