Sloped Through Wafer Vias for 3D Wafer Level Packaging

Deniz Sabuncuoglu Tezcan, Nga Pham, Bivragh Majeed, Piet De Moor, Wouter Ruythrooren and Kris Baert
IMEC vzw
Kapeldreef 75 B-3001 Leuven Belgium
Tel: + 32 16 28 8741 Email: Deniz.SabuncuogluTezcan@imec.be

Abstract
Through silicon via (TSV) technology is one of the critical and enabling technologies for 3D chip stacking. Many TSV approaches that have been demonstrated are application specific; and there is a great need for generic solutions. This work describes the design, fabrication and characterization of a TSV technology for silicon substrates where the interconnects are fabricated typically after standard CMOS processing and can be applied to any silicon based technology.

This so-called 3D Wafer Level Packaging (3D-WLP) technology die stacking is based on a the thinning first, via last approach: the via is fabricated from the backside of a thinned wafer. Plasma etching of the wafer is used to achieve sloped profile which allows the conformal deposition of the dielectric layer and copper seed metallization. The vias are isolated from the substrate using polymer dielectrics; and spray coating of photoresist is used to pattern the dielectric within the vias. Electrical connection between the front and the back of the wafer is achieved by partial filling of the vias with copper. All processes employed in the fabrication of sloped through wafer vias are performed using standard wafer handling and at low temperature (< 250°C) for post CMOS compatibility.

Various dimensions of TSVs are fabricated and electrically characterized by four point measurements. The measurements and calculations on daisy chains connecting a number vias in series show that the via resistance is in the range of 20-30mΩ depending on the via size. We believe that this generic 3D-WLP via approach is suitable for many 3D applications.

Introduction
Based on the type of manufacturing platform, IMEC is developing different types of 3D integration [1]. When starting to process 3D interconnects on finished device wafers (CMOS or other), wafer level packaging technologies are used. Two different integration technologies are followed: ultra thin chip embedding and die stacking. In the latter option, TSVs are combined with (micro-)bumps in order to construct a wedding-cake type of 3D stack containing thin dies (Figure 1). This paper describes the through wafer via process required for the die stacking in the 3D-WLP integration.

The benefits of 3D architectures with TSV technology for future ICs include reduced interconnect delay due to shorter chip to chip interconnection lengths, smaller die size which is motivated by the portable and hand held applications, and ability to use distinct, even heterogeneous technologies (analog, logic, RF, MEMS, SiGe, III-V) on separate vertically interconnected layers to build complex systems.

Figure 1. Scheme of the wedding-cake type of die stacking approach in the 3D-WLP integration.

Currently, there are a variety of ways to compactly connect multiple chips using peripheral wiring technologies; however, through wafer vias are required for the highest interconnect density. Applications for TSV in ICs include providing ground for a single chip to its package and making a low impedance connection to a backside common ground, e.g., to reduce parasitic in RF circuits or to protect sensitive analog sections of a mixed signal chip from noisy digital circuits. For high density sensor arrays, such as focal plane arrays, TSV serve to move electrical wiring away from the sensor side to allow for higher fill factors. When combined with wafer bonding or flip chip technology, electrically connected stacks of multiple chips are possible, like memory stacks. For all these applications, through silicon vias with diameters between 30µm and 150µm are sufficient [2].

One critical aspect of such a technology is the realization of reliable through wafer vias. In the through wafer via processing, our approach differs significantly from what others are pursuing. Instead of straight walled vias, we have developed a sloped via etch process to ensure void free, conformal deposition of insulation and copper seed layers. Moreover, polymer dielectric is used as passivation of the silicon in place of silicon oxide or nitride; while the vias are only partially filled with copper for electrical connection. Advantages of this strategy include: easier patterning inside or close to the vias (compared to vertical via walls), fast electroplating of the copper (compared to bottom-up filling) and reduced stress concentrations (compared to silicon oxide or nitride dielectrics and fully copper filled vias).

Furthermore, wafer thinning is used to reduce the need for high aspect ratios, making via etching and thin film deposition easier. Since, thin wafers are too delicate to handle in standard semiconductor processing equipment, processing on carrier wafer is mastered.

In the present work, a wafer thickness/via depth of 100µm has been targeted with partial filling to realize a void free copper via for implementation in 3D integrated systems. The sloped vias are fabricated typically after standard CMOS processing, requiring virtually no changes to the original device process and making it an inherently generic approach where diameter size can be large and low aspect ratios can be tolerated. It is a “circuit first” methodology, and as the key
feature, is compatible with standard bulk silicon IC wafers, such as those produced by standard CMOS foundry.

This paper describes the technology development for the sloped through wafer vias in thinned silicon ICs. These 3D interconnects are processed post chip passivation and allow low to medium interconnect density (10-100/mm²) [3].

Fabrication

Figure 2 shows the schematic wafer level process flow for the sloped through silicon vias. We start with 200mm standard silicon wafers, which have a 200nm silicon oxide and 1µm thick patterned aluminum layer on the front to simulate a standard IC wafer. At the beginning of the via processing, the silicon device wafer is mounted face down on a glass carrier using wax as a glue layer (Figure 2(a)). Acetone solvable glue, Quickstick 135, is diluted and spin applied on the glass carrier wafer. Corning 7740 pyrex glass is used as carrier for its better coefficient of thermal expansion matched to silicon. The carrier and the silicon wafer are bonded using EV501 wafer level bonding tool by applying temperature and pressure in a controlled environment. The silicon wafer is then thinned down to 100µm by grinding using Disco DFG8560 with an excellent total thickness variation over a wafer of below 2µm using both coarse and fine grinding to achieve high throughput and excellent surface quality. The wafer stack is then cleaned to remove particles, and the surface damage after grinding is removed by a fluorine plasma etch step [4].

In order to pattern via mask, 15µm thick photoresist is spun and patterned on the ground wafer surface. The via areas are defined using front to back alignment in IQ Aligner from EVG. Since the device wafer is glued face down on a glass carrier, the alignment is done looking through the glass to the front side of the wafer which is a special feature of this alignment tool. The sloped via profile, shown in Figure 2(b), is achieved by reactive ion etching in an ICP tool from Surface Technology Systems by simultaneously applying etch (SF₆) and passivation gasses (C₄F₈). The details of the sloped silicon etching have been presented elsewhere [5]. The buried 200nm silicon oxide and 1µm aluminum metal contact foreseen on the wafer front serve as an etch stop layer. Further, the metal contact serves as a landing pad for the via. The target slope angle for the via walls is 75-80° which allows the conformal deposition of the following layers. The thick resist is removed and the wafers are then subjected to a maskless dry etch step (Figure 2(c)). This removes negative angles near the via top and sidewall roughness that would otherwise cause problems in the subsequent conformal coating steps as well as increase leakage currents [6].

Figure 3. Microscope views focusing on the bottom of the vias after the photoresist development showing different dimensions of parylene opening successfully defined in the photoresist.
In Figure 2(d), the silicon oxide layer is etched away by CF$_4$ plasma to expose aluminum landing pad for electrical connection. Afterwards, 1-2µm of parylene N layer is CVD deposited as a conformal dielectric layer. This parylene layer is removed over the buried aluminum contact at the bottom of the via by dry etching in an oxygen plasma (Figure 2(e)).

The patterning of the parylene is achieved by spray coating of diluted AZ 4562 photoresist. A special process with heated chuck is developed for improved corner coverage [7]. The patterning of the photoresist is again done by front to back through glass alignment to have the best alignment accuracy since after the silicon via etching the shape of the alignment marks defined in the via etch mask are destroyed and the sharp views required for alignment are lost.

Figure 3 shows the microscope views of the wafer surface focusing on the bottom of the vias after the photoresist development showing different dimensions of parylene opening successfully defined in the photoresist. Figure 4 shows the microscope view of the via bottom after parylene etching and resist removal where the exposed aluminum contact at the bottom of the via can be seen clearly.

After the photoresist removal, the copper seed layer, which is composed of 30nm titanium/300nm copper/30nm titanium, is then sputtered for the consecutive copper electroplating. Spray coating of diluted photoresist is again used at this stage to define structures for plating. Top titanium is removed just before the electroplating of the 5-20µm thick copper layer which serves as the main conductive path between the silicon wafer front and back (Figure 2(f)). Finally, the spray coated plating resist and the seed layer are removed. Optionally the vias are filled with BCB, passivating the copper lines and planarizing the wafer surface. All processes employed in the fabrication of sloped interconnects are performed at low temperature (< 250°C) for post CMOS compatibility.

Various sizes of sloped through wafer vias have been fabricated with this process. Figure 5 shows the SEM picture of a fabricated sloped via where the top diameter size is ~140µm and the bottom diameter is ~100µm. The figure proves the continuous plating of copper in the via as well as on the side walls and at the top corner of the via.

Characterization

The test vehicle used to develop the through wafer via technology includes via daisy chains of various lengths connecting different numbers of vias. Daisy chains composed of 14-18 vias in series are I-V characterized by four point measurements from the copper metallization side to extract electrical properties of the individual vias with different dimensions.

Figure 7(a) shows the schematic 3D drawing of a daisy chain composed of four vias. In order to correctly compare the individual vias in different daisy chains, we have defined a daisy chain element which is composed of a via and half of the connecting top and bottom metallization (see Figure 7(a)). Figure 7(b) shows part of a layout design of the daisy chains where the connecting copper and aluminum lines are designed with the same dimensions. The copper routing lines shown in the same picture connect the first and the last via of each daisy chain to separate bond pads to allow for probing, and hence, electrical measurements.
Figure 7. (a) Schematic 3D drawing of a daisy chain with four vias and (b) layout design showing part of a daisy chain.

Figure 8 shows the microscope view of a via processed wafer surface where the copper connection of the daisy chains and the copper routing lines are clearly seen. Before measuring the daisy chains, separate meander type structures which were designed to measure the sheet resistance values of the copper and aluminum layers are I-V characterized. Knowing the dimensions of these meanders, the sheet resistance of aluminum and copper layers are extracted from the measurements as 43mΩ/sq. and 1.8mΩ/sq., respectively. These sheet resistance values are then used to calculate the resistance of the metal lines connecting each via along the wafer front and back surface. These connecting metal resistance values are subtracted from the corresponding via chain resistance to yield the resistance of an individual via in a certain daisy chain.

I-V curves of various daisy chains corresponding to three different dimensions of vias are measured. Each of these measurements is then divided to the number of vias in the corresponding daisy chain to get resistance per daisy chain element. Figure 9 plots the results of these measurements, where each dot in the graph corresponds to a different daisy chain. This graph shows that the resistance of a daisy chain element increases while the size of the via reduces. Since the pitch of the daisy chain element is constant, this increase is mainly due to the metal interconnect lines, i.e., as the via gets smaller the metal connection lines get longer.

Figure 8. Microscope view of the wafer surface where the copper connection of the daisy chains and the routing copper lines are clearly seen.

Figure 9. Resistance per daisy chain element measurement results for three different via dimensions. Each dot in the graph corresponds to a different chain. The trend in the graph is mainly due to metal interconnect line which are getting longer as the via gets smaller since the via pitch is constant.

Furthermore, as the aluminum sheet resistance is about 24 times higher than the copper and the dimensions of the copper and aluminum connection lines are designed the same (see Figure 7(b)), the main resistance contribution in Figure 9 originates from the aluminum layer. Figure 10 plots the average individual via resistance values extracted from the values in Figure 9 by subtracting the connecting metal line resistances. In this graph, it is seen that the via resistance is typically in the range of 20-30mΩ. There is a slight increase of via resistance as the via dimensions get smaller. This is mainly due to the size of the parylene opening which is designed comparably smaller for smaller vias leading to smaller area for copper-aluminum contact.

Figure 10. Average individual via resistance values for three different via dimensions, showing that the resistance for a via is typically in the range of 20-30mΩ.

Table 1 summarizes the results presented in Figure 9 and 10 where the top and bottom diameter of the via, the average
resistance of a daisy chain element and the average individual via resistance for each via dimension are listed. As seen in this table, the resistance contribution of a via in a daisy chain is comparable or smaller than the contribution of the connecting metal lines (especially of the aluminum layer).

Table 1. Summary of the daisy chain measurement results including the via dimensions.

<table>
<thead>
<tr>
<th>Via Bottom diameter</th>
<th>60µm</th>
<th>80µm</th>
<th>100µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via top diameter</td>
<td>100µm</td>
<td>120µm</td>
<td>140µm</td>
</tr>
<tr>
<td>Resistance of dc element*</td>
<td>109mΩ</td>
<td>82mΩ</td>
<td>52mΩ</td>
</tr>
<tr>
<td>Resistance of one via**</td>
<td>30mΩ</td>
<td>28mΩ</td>
<td>24mΩ</td>
</tr>
</tbody>
</table>

* Average of daisy chains elements, including the connecting metal resistance.
** Average of individual via resistances, excluding the connecting metal resistance.

Conclusions
A generic sloped through wafer via process is developed which is applicable to any silicon technology. Various sizes of vias and different lengths of daisy chains are fabricated with this process. The daisy chains composed of 14-18 vias are I-V characterized by four point measurements and individual via resistances are extracted. Via resistances in the range of 20-30mΩ are measured. These values are suitable for many 3D applications.

Acknowledgments
EV Group is acknowledged for enabling the through glass carrier backside alignment on the EVG IQ aligner.

References