A noise aware CML latch modelling for large system simulation

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Abstract—Modern high speed communication systems often employ both analog and digital blocks. This poses a challenge for simulation of closed loop system dynamics in presence of non-idealities in any of the analog blocks. Due the size and complexity of such systems it is not possible to do full system level simulation with circuit level models. The presence of digital control blocks makes it difficult to elevate block level observations to system level performance. A major challenge is the difficulty in estimating the error rate at the output of digital latches (continuous-time to discrete-time domain crossing boundaries) in the presence of noise and non-ideal analog input signals. Simplistic models used currently are often inadequate in capturing the long term effects of non ideal behavior at the block level. In this paper we propose a simulation framework to estimate latch transition probabilities in the response to distorted input and clock waveforms in presence of white noise. The evaluated transition probabilities are then used to estimate system performance using an illustrative example.

Index Terms—

I. INTRODUCTION

Mixed signal systems, incorporating both digital and analog components, are hard to simulate. The analog blocks in the system require high resolution time domain simulation with detailed device models, while the digital systems work in the discrete time domain with finite levels. To reduce the simulation effort, simplified behavioral models of the system blocks are used with idealized waveforms. A major challenge in simulation of such systems is to reconcile the two distinct time domains : continuous-time analog vs discrete-time digital with latches and flip-flops at the domain crossing boundaries. A common approach to emulate such domain crossing is to model the latch as a perfect two valued quantizer, that compares the value of the input at a given (infinitely sharp) clock edge with a threshold and produces a digital output. While such simulation frameworks can provide reasonable accuracy for determining nominal timing margins in the system, they fail to capture the effects of noise and other non ideal behavior. This makes estimation of the effect of an observed deviation in the signal waveform at any of the inputs of the latch or the clock signal at the system level a difficult proposition.

Inability to estimate the effects of non ideal waveforms in the analog domain on system performance severely limits the ability to fix design margins since one can not determine if a certain deviation can lead to a failure at the system level or can be observed by the test suite. To be able to accurately estimate such effects, we need a model that can take an initial probability distribution of the node voltages of the latch and evolve it through time to the end of a transient in the clock edge. Such a model is conceptually shown in Fig. 1. The inputs to such a model are the input waveforms $u(t)$, and clock waveforms $ck(t)$ and an initial probability distribution $p(x, 0)$ where $x$ is the state space defined by the node voltages, and the noise power at the internal nodes $\{\sigma\}$. The model then integrates the effect of the noise through the clock edge transient in the metastable region of the latch and outputs the final probability distribution $p(x, t_{end})$. For practical reasons, the noise is assumed to be white noise. [1].

One way of solving such a problem is to do Monte-carlo simulations to simulate multiple scenarios in the presence of noise with a reduced order dynamic model. However a more efficient way is to obtain the associated deterministic equations [1] for the evolution of the probability density from the reduced order dynamic model and solve it in time. In this paper we take the latter approach. A benefit of such an approach is considerable reduction of the simulation effort.

Once the final probability density is calculated it can be used to evaluate the probability of a ‘1’ or a ‘0’ or an indeterminate state by integrating the probability density over appropriate regions of the state space. The given probability values can then be used in the system simulation by building state transition trees with each branch having an associated probability. Branches in the state transition diagram can be dropped when the probability of a given branch falls below a certain predetermined threshold. The proposed system simulation framework is shown in the flowchart presented in Fig. 2.

The main contributions of this work are:
• Development of a new approach to dynamic modeling of latches for fast mixed-signal system simulation
• Development of a model that can incorporate both noise and non ideal input waveforms
• Proposing a new framework for simulation of digitally assisted analog systems

To the best of knowledge of the authors this is the first time a Fokker-Plank based stochastic simulation is applied to a bistable latch circuit to estimate transition probabilities and apply the technique to a mixed signal system simulation flow that can preserve the impact of non-ideal waveform at the latch inputs.

The rest of the paper is organized as follows: In section II we will review the state of the art followed by a discussion of the theoretical basis of the proposed modeling approach in section III. In section IV, we will take up a simple example and apply the proposed modeling technique to it. In section V we present results followed by conclusions.

II. PREVIOUS WORK

As mentioned before, the modeling of latch metastability dynamics is extremely important. However, most of the modeling till now has focused on determining the probability of a latch staying in the metastable state after a fixed time from an ideal clock transition. A simple model of a latched comparator is shown in Fig. 3. $x_{1,2}$ are the node voltages that determine the phase space and $u_{1,2}$ are the two differential inputs. The non overlapping clock phases $\phi_1$ and $\phi_2$ alternatively switch the comparator between a tracking phase and a regenerative phase. In the tracking phase, the state of the internal nodes track the input setting an initial condition while in the regenerative phase the initial condition is resolved through a metastable region into the final latch values. Most of the initial research on latch metastability modeled the regenerative inverters as linearized small signal trans-conductances with adequate capacitor loading at the output nodes. This treatment gives rise to a simple exponential growth model in the regenerative phase [2], [3]. In [4], the model was enhanced to account for the effects of miller capacitance. The linearized model is unable to track the voltage dynamics in the regenerative phase as the voltage grows large and hence the non-linear effects are ignored. In [5], the authors incorporated this non-linearity to improve the accuracy of the model. A very general analysis of latch dynamics was presented in [6].

However all the models mentioned so far are ideal in the sense that they neglect the effects of the noise or mismatch. One such study of the effect of mismatch on metastability dynamics was presented in [7]. More recently a probabilistic approach to explaining metastability in presence of noise is used. An error probability calculation using total input referred noise at the sampling clock was proposed in [8]. A linear time varying model was used to describe the basic underlying latch dynamics.

A more accurate modeling approach was proposed in [9]. In this research the behavior in the regenerative phase was accurately modeled by a stochastic dynamic equation (SDE) and the trajectory mean and standard deviation was calculated by integrating the SDE. A similar SDE based approach was also adopted in [10] and had the important observation that a single point input referred noise may not be an accurate representation of the metastability.

The present available approaches fail to model the effects of non ideal clock edges and input waveforms. Such effects are significant in high speed current mode logic (CML) circuits. In this paper we present a more general model of the regenerative phase of a latched comparator using a SDE based approach. In order to capture the effects of non ideal clock edges, we assume that the inverter response is a general non-linear
function of the state variables and the latch inputs. A more
detailed discussion of the proposed model is presented in the
next section.

III. PROPOSED MODEL

The proposed model for simulating the transition behavior of
a latch in the regenerative phase is shown in Fig. 4. It is a
more generalized version of the model presented in Fig. 3.

Fig. 4: Improved latch model for simulation

The ideal switched inverters are replaced by more general
nonlinear current functions \(g_{11}, g_{12}, g_{21}, g_{22}\), which are
dependent on the input, output and clock waveforms. It must
be mentioned here that in the case of general nonlinear
models for the current functions, simple closed form analytical
solutions usually do not exist and the signal values must be
calculated through numerical simulations. This implies that
reduced order models for the current functions \(g_{ij}\) need to
be constructed before simulation. We also point out that the
reduced dimensional models may have inaccuracies and in
those cases where higher accuracy is required, the state model
needs be expanded to higher dimension, to include higher
order derivatives. The trans-conductance models themselves
can be constructed by model order reduction from nominal
simulations over the space of the observed input waveforms
which includes the output obtained from simulation of the non
ideal analog blocks. There are many well known techniques
[11], [12] that can be used to build such models. However in
this paper we will use a simpler model as an example.

To further generalize, white noise sources, \((\eta_1, \eta_2, \eta_3, \eta_4)\)
with power levels \((\sigma_1, \sigma_2, \sigma_3, \sigma_4)\) are included. All the noise
sources are assumed to be independent. The load impedances,
\((Z_{L1} \text{ and } Z_{L2})\) are modeled by a parallel combination of resistances
\((R_1 \text{ and } R_2)\) and capacitances \((C_1 \text{ and } C_2)\) respectively.
Under these assumptions, the SDE governing the dynamics of
the latch is given by:

\[
\begin{align*}
\mathrm{dx}_1 &= -\frac{1}{C_1} (g_{11}(x_2, x_1, c_k) + g_{21}(u_1, x_1, c_k) + x_1/R_1) \, dt \\
&\quad + \sigma_1 \, d\eta_3 + \frac{1}{C_1} \frac{\partial g_{21}}{\partial u_1}(u_1, x_1, c_k) \sigma_1 \, d\eta_1 \\
\mathrm{dx}_2 &= -\frac{1}{C_2} (g_{12}(x_1, x_2, c_k) + g_{22}(u_2, x_2, c_k) + x_2/R_2) \, dt \\
&\quad + \sigma_4 \, d\eta_4 + \frac{1}{C_2} \frac{\partial g_{22}}{\partial u_2}(u_2, x_2, c_k) \sigma_2 \, d\eta_2
\end{align*}
\]

(1)

If required, noise sources can also be considered in the clock
clock, by using a first order perturbation about \(c_k\). In order to
solve the set of SDE given in 1, numerically, a large numerical
effort is required. Instead of solving the set of dynamic
equation directly it is computationally more manageable to
solve for the evolution of probability density function (pdf)
in the state space. The dynamics of the evolution of the pdf
of the state space for such a system is given by the Fokker-
Planck equation (FPE) [1]. For the model under consideration,
the FPE can be written as:

\[
\frac{\partial p(x_1, x_2, t)}{\partial t} = \frac{\partial}{\partial x_1} (\mu_1 p(x_1, x_2, t)) + \frac{\partial}{\partial x_2} (\mu_2 p(x_1, x_2, t)) \\
+ \frac{4}{\partial x_1^2} D_{11} p(x_1, x_2, t) \\
+ \frac{4}{\partial x_2^2} D_{22} p(x_1, x_2, t)
\]

(2)

where,

\[
\mu_1 = \frac{1}{C_1} (g_{11}(x_2, x_1, c_k) + g_{21}(u_1, x_1, x_2, c_k) + x_1/R_1)
\]

\[
\mu_2 = \frac{1}{C_2} (g_{12}(x_1, x_2, c_k) + g_{22}(u_2, x_1, x_2, c_k) + x_2/R_2)
\]

\[
D_{11} = D_{22} = 1
\]

\[
D_{33} = \frac{1}{C_1^2} \frac{\partial g_{21}}{\partial u_1}(u, x, c_k) \frac{\partial g_{21}}{\partial u_1}(u, x, c_k) \]

(3)

and < \eta_i ^2 > = \sigma_i ^2 dt is the power spectral density of the noise.
For more diverse noise sources with mutual correlation, the
term in second order spatial (not real space variable but with
respect to the phase space) derivatives would be:

\[
\sum_{i=1}^{4} \sigma_i \sigma_j r(i, j) \frac{\partial^2}{\partial x_i \partial x_j} D_{ij} p(x_1, x_2, t)
\]

(4)

where, \(r(i, j)\) is the correlation coefficient of the noise sources
indexed \(i \text{ and } j\) respectively, with \(D_{ij}\) being the appropriate
coupling term for example for noise source 3 and 4 the cross
term will be,

\[
D_{34} = \frac{\partial g_{21}}{\partial u_1}(u, x, c_k) \frac{\partial g_{22}}{\partial u_2}(u, x, c_k)
\]

The equation has two parts, a drift part with first order
spatial derivatives which represent the noise free dynamics of
the system and a diffusion part which represents the scattering
effects of the noise. In the general nonlinear case, the FPE does
not have a closed form analytical solution. Which means that
the equation should be solved numerically. Solving the FPE
explicitly reduces the error in estimation since it can handle
cases where the final pdf is not necessarily a Gaussian and
also inherently accounts for the effects of non ideal input
and clock waveforms. For a numerical solution of the FPE,
the trans-conductance functions used need not be expressed
in closed form and can be defined only at discrete points in
the state space, with piece wise smooth, continuous function.
The values at the intermediate points can be calculated using
interpolation techniques.

The initial condition can be set from the solution at the end of a previous clock cycle or by assuming a pure ‘1’ or ‘0’
state as a Dirac delta function \( p(x_1, x_2, 0) = \delta(x_1 - 1, x_2) \) and \( p(x_1, x_2, 0) = \delta(x_1, x_2 - 1) \) respectively. Once the numerical solution of the FPE is obtained by solving (2) using the initial condition \( p(x_1, x_2, 0) \) up to the end of the available time \( t_{avl} \), we can integrate the pdf to obtain the probability of a ‘1’ or a ‘0’ as

\[
P(1) = \int_{V_{th,h}}^{V_{th,l}} p(x_1, x_2, t_{avl})dx_1 \quad \text{(5a)}
\]
\[
P(0) = \int_{V_{th,d}}^{V_{th,h}} p(x_1, x_2, t_{avl})dx_1 \quad \text{(5b)}
\]

Where \( V_{th,h} \) and \( V_{th,l} \) represent the high and low logic threshold. Once the probabilities in (5) are known they can be used to construct the state transition diagram for the digital finite state machine. The proposed simulation framework allows one to promote the effects of non-ideal response at the analog blocks through the continuous time - discrete time domain crossing and evaluate the effects at a system level.

In the next section we apply the concepts presented in this section to a CML latch model.

**IV. EXAMPLE: CML LATCH MODELING**

In this section we apply the concepts from section III, to a CML latch as an example. The basic CML latch circuit is shown in Fig. 5. The CML latch is chosen over a CMOS latch because of the higher speed of operations of a CML circuit compared to a CMOS circuit. For simplicity we will assume that the circuit has no mismatch and that the noise on the two nodes have equal power density and is small. This implies that the circuit will operate under differential conditions and the time varying part of the common mode signal given by \( V_{cm} = \frac{1}{2}(x_1 + x_2) \) will be small. This makes it feasible to consider the ac component of the signal by removing the dc common mode, and considering the excursion of \( x_1 \) and \( x_2 \) about this dc value. We will also assume that the output impedance of all the transistors can be neglected in comparison with the individual drain loads.

Also the total current is limited by design to \( I_{tot} \). The clock signal controls how much of this current flows in the buffer and the rest goes into the regenerative pair. Again neglecting the common mode of the clock signal, and considering only the differential mode of the clock signal \( ck \), we can write,

\[
I_{buf} = s_1(ck)I_{tot}
\]
\[
I_{reg} = (1 - s_1(ck))I_{tot}
\]

for the two branches of the current with \( s_1(ck) \) being the shaping function representing transfer characteristics of the differential pair driven by the clock. It varies from 0 to 1 as clock waveform varies from \(-V_{ck}\) to \(+V_{ck}\) and shows saturation at both ends with linear dependence for small signal values. The linear trans-conductance of the differential pair for small inputs being equal to:

\[
\frac{g_{m,ck}}{4V_{ck}} = \frac{\pi}{4V_{ck}}I_{tot}
\]

or,

\[
V_{ck} = \frac{\pi}{4 \left( \frac{g_{m}}{I_{tot}} \right)} = \frac{\pi}{2 \left( \frac{g_{m}}{I_{tot}} \right)}
\]

For the upper differential pair driven by the inputs, the tail current is limited to \( I_{buf} \). The differential voltage \( u_1 - u_2 \) causes the current to commute between the \( x_1 \) and the \( x_2 \) nodes. For small values of differential inputs, the linear trans-conductance for each branch is given by:

\[
\frac{g_{m,buf,lin}}{2k_n \left( \frac{W}{L} \right)} \frac{I_{buf}}{2}
\]

so that the current for the two branches are given by:

\[
i_{1, buf} = g_{m,buf,lin} \times (u_1 - u_2)/2
\]
\[
i_{2, buf} = g_{m,buf,lin} \times (u_2 - u_1)/2
\]

However for large inputs, maximum current commutation occurs and the current in each branch is limited to \( \pm \frac{I_{buf}}{2} \). The saturation occurs as the input voltage becomes comparable to:

\[
(u_1 - u_2)/2 \approx \frac{I_{buf}}{2} \times \frac{1}{g_{m,buf,lin}}
\]

or,

\[
|u_1 - u_2| \approx \sqrt{\frac{I_{buf}}{2k_n \left( \frac{W}{L} \right)}}
\]

![Fig. 5: Schematic of a CML latch](image-url)
For this experiment we smooth the slope discontinuity by using a moving average filter. A more exact model can be easily reconstructed by plotting the output current vs the input voltage as the tail current is varied from an exact simulation. The equations for the regenerative circuit is similar with \( u_1 \) and \( u_2 \) replaced by \( x_2 \) and \( x_1 \) respectively. For the regenerative branch we can write:

\[
\begin{align*}
    g_{m,\text{reg,lin}} &= \sqrt{2k_n \frac{W}{L} \frac{I_{\text{reg}}}{2}} \\
    i_{1,\text{reg}} &= g_{m,\text{reg,lin}} \times (x_2 - x_1)/2 \\
    i_{2,\text{reg}} &= g_{m,\text{reg,lin}} \times (x_1 - x_2)/2
\end{align*}
\]

The current in each branch being limited to \( \pm \frac{I_{\text{reg}}}{2} \) with saturation applied to the input,

\[
|x_2 - x_1| \approx \sqrt{\frac{I_{\text{reg}}}{k_n \frac{W}{L}}}
\]

Again we assume a smooth transition between the linear and the saturation regimes and apply a moving average filter to the i-v transfer characteristics.

For the noise perturbation we assume a direct equivalent noise excitation at the output nodes \( x_1 \) and \( x_2 \) with standard deviation \( \sigma \). We neglect the other noise voltages for this example. Also the parallel \( R \) and \( C \) is assumed as a load at each of the output nodes. So the SDE governing the dynamics can be written as:

\[
\begin{align*}
    \frac{dx_1}{dt} &= -\frac{1}{C} \left( i_{2,\text{buf}} + i_{2,\text{reg}} + \frac{x_1}{R} \right) dt + \sigma d\eta_1 \\
    \frac{dx_2}{dt} &= -\frac{1}{C} \left( i_{2,\text{buf}} + i_{2,\text{reg}} + \frac{x_2}{R} \right) dt + \sigma d\eta_2 \quad (8)
\end{align*}
\]

in this equation \( \eta_1, \eta_2 \) are unit power white noise process, so that the relevant FPE is given as:

\[
\begin{align*}
    \frac{\partial p}{\partial t} &= \frac{1}{C} \left( \frac{\partial}{\partial x_1} \left( i_{2,\text{buf}} + i_{2,\text{reg}} + \frac{x_1}{R} \right) p \\
    &+ \frac{1}{C} \left( \frac{\partial}{\partial x_2} \left( i_{2,\text{buf}} + i_{2,\text{reg}} + \frac{x_2}{R} \right) p \\
    &+ \sigma^2 \left( \frac{\partial^2}{\partial x_1^2} + \frac{\partial^2}{\partial x_2^2} \right) p \quad (9)
\end{align*}
\]

V. SIMULATION RESULTS

For the simulation, realistic values for noise levels, impedance and operating points are calculated from a reference design designed in 180 nm CMOS to work upto 10 Gbps. The \( I_{\text{tot}} \) is taken to be 3.9 mA and the operating point of the transistors are taken to be such that ratio of trans-conductance to quiescent drain current is \( g_m/I_{\text{d}} = 4 \) for the clock switching transistors and \( g_m/I_{\text{d}} = 3 \) for the differential pairs for both the buffer and the regenerative transistors for the maximum tail current condition. The load resistance is taken to be \( R = 200\Omega \) and load capacitance \( C = 90f\text{F} \). The resultant current curves with varying clock voltage is shown in Fig. 6. The FPE is a conservation law for the probability density function. Also the model calls for possibility of sharp edges (e.g. asymptotically stable state trajectories). Hence a high accuracy scheme with low numeric dissipation should be used. A good choice for such a system are the “monotone upstream-centered schemes for conservation laws” (MUSCL) based schemes. The semi-discrete formulation proposed by Kurganov and Tadmor [13] is used for each direction. For the time integration a forward Euler integration is used.

Due to the small accuracy of the forward Euler integration the time step is chosen to be 2 orders of magnitude smaller than that required by the CFL condition for stability.

To demonstrate the capability of the technique a sinusoidal input and a finite slew clock is used. The clock and the signal waveform are shown in Fig. 7. It is simulated with an initial
Fig. 8: Contour plot of evolution of probability through time in absence of noise at 0, 20ps, 40ps and 60ps; x and y axes represent the two states of the system

solution as $P(1) = 0.19$ and $P(0) = 0.81$.

Fig. 9: Contour plot of evolution of probability through time with noise at 0, 20ps, 40ps and 60ps; x and y axes represent the two states of the system

The variation of transition probability phases for the four phases as we sweep the clock over a period of 1010... data (two clock period), is shown in Fig. 10. The variation of the transition probabilities with clock slew rate is shown in Fig. 11.

A. Application to system simulation: example

The above model is applied to simulate the dynamics of a clock phase recovery loop using a binary phase detector. This can be used in systems where a data clock is forwarded over long traces and accumulate phase skew. To correct the phase skew a phase rotator based system can be used to acquire the clock phase as shown in Fig. 12. The signal is sampled at three phases early(e), center(c), and late(l) separated by half the clock period as shown in Fig. 13. The state machine is described as:

$$
\phi \leftarrow \phi + 1 \text{ if } [e, c, l] = 110 \text{ or } 001 \\
\phi \leftarrow \phi - 1 \text{ if } [e, c, l] = 100 \text{ or } 011 
$$

(10)

where $\phi$ is the index of discrete phase (offset) state that the system can be in. The corresponding state transition diagram is shown in Fig. 14.

The incoming data will have a finite transition probability given by $p(+e)$ and $p(-e)$ for positive and negative transition probabilities from a 0 and a 1 respectively. The steady state mark density of the data must then be given by:

$$
p_{\text{data}}(1) = \frac{p(+e)}{p(+e) + p(-e)} \\
p_{\text{data}}(0) = \frac{p(-e)}{p(+e) + p(-e)}
$$
The dynamics of the state probabilities neglecting drift due to clock phase noise is given by the following set of equations

\[
\begin{align*}
\{d_1d_2d_3 - d_1'd_2'd_3'\} & \equiv p(e, \phi, \{d_1d_1'\}) \quad p(e, \phi, \{d_2d_2'\})p(e, \phi_1, \{d_3d_3'\}) \quad (11)
\end{align*}
\]

written in compact form:

\[
\begin{align*}
p^n(e, \phi, d_1d_2d_3) &= [p^{n-1}(ne, \phi, 111\{111 - d_1d_2d_3\}) + p^{n-1}(ne, \phi, 010\{010 - d_1d_2d_3\}) + p^{n-1}(ne, \phi, 101\{101 - d_1d_2d_3\}) + p^{n-1}(ne, \phi, 000\{000 - d_1d_2d_3\}) + p^{n-1}(ne, \phi - \phi, 011\{011 - d_1d_2d_3\}) + p^{n-1}(ne, \phi + \phi, 110\{110 - d_1d_2d_3\}) + p^{n-1}(ne, \phi + \phi, 001\{001 - d_1d_2d_3\})] p(ne|e) \\
&\quad + [p^{n-1}(+e, \phi, 111\{111 - d_1d_2d_3\}) + p^{n-1}(+e, \phi, 010\{010 - d_1d_2d_3\}) + p^{n-1}(+e, \phi, 101\{101 - d_1d_2d_3\}) + p^{n-1}(+e, \phi, 000\{000 - d_1d_2d_3\}) + p^{n-1}(+e, \phi - \phi, 011\{011 - d_1d_2d_3\}) + p^{n-1}(+e, \phi + \phi, 110\{110 - d_1d_2d_3\}) + p^{n-1}(+e, \phi + \phi, 001\{001 - d_1d_2d_3\}] p(+e|e) \\
&\quad + [p^{n-1}(-e, \phi, 111\{111 - d_1d_2d_3\}) + p^{n-1}(-e, \phi, 010\{010 - d_1d_2d_3\}) + p^{n-1}(-e, \phi, 101\{101 - d_1d_2d_3\}) + p^{n-1}(-e, \phi, 000\{000 - d_1d_2d_3\}) + p^{n-1}(-e, \phi - \phi, 011\{011 - d_1d_2d_3\}) + p^{n-1}(-e, \phi + \phi, 110\{110 - d_1d_2d_3\}) + p^{n-1}(-e, \phi + \phi, 001\{001 - d_1d_2d_3\}] p(-e|e) \quad (12)
\end{align*}
\]

where, \(p(ne/ +e/ -e|e)\) is the probability that in the last clock cycle, there was one positive edge or a negative edge given that the current clock there is a edge of type \(e\) respectively. The phase noise of the clock will be given by the steady state solution of the equation (12) obtained by setting \(p^n(\cdot) = p^{n-1}(\cdot)\). Also, \(p(e, \phi, d) = p(d(e, \phi)p(e)p(\phi)\) and \(p(e, \phi, d_1d_2d_3) = p(d(e, \phi - \pi)p(d_2d_3)e)p(d_1\{e, \phi + \pi\})p(e)p(\phi)\)

Now it can be assumed that the state space of the PLL is divided into \(4N\) discrete phases. For each of the index \(c\), the transition probabilities can be evaluated as:

\[
\begin{pmatrix}
\bar{p}^r[0,0] \\
\bar{p}^r[0,1] \\
\bar{p}^r[1,0] \\
\bar{p}^r[1,1]
\end{pmatrix}
\]

by using the proposed model starting with appropriate initial condition. It is also worth mentioning that the transition probabilities are independent of time as long as the input and clock waveforms remain same. Once the transition probabilities are evaluated, the expression in (12) can be used to evaluate the state transition diagram of the state transition after each time period. The mode and standard deviation of the phase dynamical behavior starting from a point initial condition is shown in Fig. 15 and Fig. 16.
VI. CONCLUSIONS

We have proposed a novel technique of modeling latches that can emulate the effect of non-ideal input and clock waveforms. The technique first relies on deriving the reduced order noise free model of the latch followed by the inclusion of noise effects in the form of a stochastic differential equation. Even though in this paper a simple hand built model is used for simplicity, in real system the model building can be automated by using techniques referred to in the paper.

From the SDE the Fokker-Planck equation (FPE) is derived for the probability density evolution in time. The FPE is then solved numerically to derive the appropriate transition probabilities. Which can be then used to evaluate a state dynamics of a discrete time digital system that is excited by the output of the latch. An example is provided with a qualitative analysis of a CMOS latch and how it can be adapted to a system simulation. To the best of the knowledge of the authors, this is the first time such a simulation framework is proposed. This can lead to significant improvement in time and accuracy in simulating systems with both continuous time and discrete time components.

REFERENCES