Nonlinear Function Controller: A Simple Alternative to Fuzzy Logic Controller for a Power Electronic Converter

Kanakasabai Viswanathan, Member, IEEE, Ramesh Oruganti, Senior Member, IEEE, and Dipti Srinivasan, Senior Member, IEEE

Abstract—Recently, there has been an increase in the application of fuzzy logic controllers (FLCs) for control of power electronic converters. Due to the FLCs’ complex algorithm, their realization often calls for a compromise between cost and performance. In this paper, it is shown that the rule table of most of the two-input FLCs used with power converters can be approximated into a single nonlinearity. This allows the controller to be easily realized using simple, fast, and inexpensive analog circuits. The simplified “nonlinear function controller (NLFC)” developed in this manner is shown to be equivalent in performance to the original FLC through simulations. The NLFC concept is then applied to PI-FLC, a type of FLC popular in power converter control applications. This results in the PI-FLC being replaced by a simple “nonlinear PI controller (NPIC).” Using this simplification, the design of NPICs to obtain good dynamic performance in power converters is explained. An example design of NPIC for controlling a dc–dc boost power converter is presented. Experimental results are also presented to demonstrate the superior dynamic performance of the converter with NPIC versus that of a linear-PI controller.

Index Terms—Dynamic response, fuzzy control, fuzzy logic, pulsewidth-modulated (PWM) power converters, switched-mode power supplies, Toeplitz matrices.

I. INTRODUCTION

RECENTLY, there have been several publications which apply fuzzy logic controllers (FLCs) to control power electronic converters [1]–[14]. In general, these nonlinear controllers have been shown to offer excellent dynamic response in power converters [1], [4], [7], [8], [10], with [1] and [7] demonstrating, in particular, the excellent large-signal dynamic response characteristics offered by FLCs. One of the major problems with an FLC is its complex algorithm that often makes its realization a challenging task.

In this paper, based on an investigation on the input/output sets and rule bases of several FLCs used to control power electronic converters [1]–[14], it is shown most FLC rule tables can be approximated using single-input-single-output (SISO) nonlinear functions. The motivation behind this simplification comes from [15], in which the reduction of a two-input FLC with a certain type of rule table into a single-input FLC is described. The main advantage of such a simplification is that converter performance identical to that using an FLC can be obtained using very simple nonlinear control circuitry without the use of complex implementations.

With this simplification in place, it would be more appropriate to call the implemented controller a “nonlinear function controller (NLFC)” than as a “fuzzy logic controller (FLC).” The proposed NLFC and the conventional FLC are nearly equivalent in their control performance capability and are virtually interchangeable. Besides simplified implementation, the proposed controller has several other advantages. The simplified structure of the NLFC makes it easier to explain the better large-signal performance obtained typically with FLCs when compared to that obtained with linear controllers. Besides, the process of designing NLFCs (and indeed FLCs) to yield good small-signal dynamic performance similar to linear controllers becomes logical.

In this paper, reduction of a two-input FLC rule table of the type typically used in power converter control applications into an NLFC is described in Section II. Following this, simplification of a PI-FLC [10], a type of FLC popular in power converter control to nonlinear PI controllers (NPICs), which is a type of NLFC, is presented in Section III. The structural similarity between the NPIC and the linear-PI controller is discussed, based on which design of the NPIC and hence PI-FLCs to offer excellent dynamic performance in power converters is described. Simulation results based on step disturbances on a single-switch dc–dc boost power converter are presented to validate the replacement of PI-FLC by NPIC (Section IV). An experimental prototype of the NPIC has been designed, built, and tested on the converter. Experimental results demonstrating the superior performance offered by NPIC over a linear-PI controller are presented in Section V.

II. ANALYSIS OF FLC STRUCTURE POPULAR IN POWER CONVERTER CONTROL

In this section, the structure of several FLCs that have been used to control power converters in literature are investigated, based on which a simple nonlinearity that approximates the fuzzy rule table is presented. A simple analog circuit that replaces the FLC itself is also presented.
A. Shape of Membership Functions and Fuzzy Operators

The first stage in all FLCs is the fuzzification of the inputs. The FLCs proposed in [1]–[7], and [9]–[13] take error and change in error of the output state as inputs. Reference [8] proposes an FLC for buck-boost and Sepic converters, in which the inputs are the output voltage error and the inductor current error. In all of the above cases, the shape of all of the input membership functions other than those at the extreme ends of the range are triangular [refer to Fig. 1(a)] and have a 50% overlap. The triangular membership functions are symmetric in [1]–[3], [7], [8], [10], and [13] and asymmetric in [4], [5], and [11].

The output membership functions are either singletons, as in Sugeno-type FLCs [Fig. 1(b)] [1], [2], [9], [10] or triangular/trapezoidal with 50% overlap [Fig. 1(c)], as in Mamdani-type FLCs [3]–[5], [7], [8], [11], [12]. The membership functions are asymmetric triangles in [5] and [11].

The membership grades of the output membership functions are generally determined either by Mamdani’s minimum fuzzy implication or by Larsen’s product implication [19]. Among the several defuzzification methods [19], the centroid method is widely used [1]–[4], [6], [10], [11].

Considering an FLC with triangular (symmetric or asymmetric) input and output membership functions having 50% overlap, the input–output relation can be expressed as a fuzzy associative memory (FAM). Irrespective of the different fuzzy operators and implications, FLCs having the same FAM will give the same output for the inputs at which the rules are defined in the FAM (rule table). This fact is used in the proposed simplification.

B. Rule Base Structure

The heart of an FLC is the rule/knowledge base represented by FAM. In this subsection, the rule bases of several FLCs implemented with power converters are examined. It is seen that, in most of the cases, the rule base has a Toeplitz [18] structure. In most of the other cases, the rule base is found to be near-Toeplitz. Such a Toeplitz structure of the rule base leads to the simplification of FLC proposed in this paper.

Table I shows a Toeplitz rule base with output memberships constant along each (top-left to bottom-right) diagonal. Here, \( x_1 \) and \( x_2 \) are the FLC inputs. Such an exact Toeplitz rule base has been used in [3]–[7], [9], [11], and [12].

The rule tables in [13] and [14] have a near-Toeplitz structure with only four violations out of 49 rules. Information about the rule table structure in [10] is not available.

The rule tables of fuzzy-P and fuzzy-I controllers in [8] are near-Toeplitz with violations at the extreme ends when the output voltage error becomes too large (PL or NL).

The rule base of Sugeno-type FLCs used in [1] and [2] is shown in Table II. It may be noticed that this rule table does not have an exact Toeplitz structure, as the elements in the top-left-to-bottom-right diagonal are not identical. However, by extending the range of \( x \) input and increasing the granularity of the rule table such that the line shown in Table II becomes the leading diagonal, the rule table can be shown to have a near-Toeplitz structure.

Hence, it may be concluded that almost all of the FLC rule tables that have been used with power converter control applications have a Toeplitz or a near-Toeplitz structure. Besides being Toeplitz, the rule tables in most of the cases are also skew-symmetric, i.e., the output membership function values along the leading diagonal of the rule table are zero-valued and those on either side of this diagonal take opposite signs (\( a_{ij} = -a_{ji} \), where \( a \) is the rule table and \( a_{ij} \) is the output membership function along the \( i \)th row and \( j \)th column).
that represents the signed distance of the par-

plane to the corresponding singleton (member-

ship) value \( r \) [Fig. 2(c)]. Consequently, the output of the FLC is

given by

\[
\mathbf{r} = \psi(\mathbf{d}).
\]  

(3)

Thus, the two-input FLC rule table is reduced to a SISO

NLFC. It must be noted that this simplification is based on linear

interpolations of the output membership functions in the rule

table. Hence, it is only an approximation of the FLC rule table

with close matches at the vertices (rules) defined in the rule

table. As FLCs themselves are based on expert knowledge that

is not quantified, such an approximation may be justified.

An odd nonlinearity like the one in Fig. 2(c) is obtained by

simplifying a skew-symmetric rule table. In the case of a rule

table not being skew-symmetric but being a Toeplitz matrix

(with zero diagonal), simplification is still possible. However, the

resulting nonlinearity will not have an odd symmetry [Fig. 2(d)].

D. NLFC: Economical and Fast Alternative to “FLC” Rule

Table and Its Circuit Realization

The reduction of multi-input rule table into a single nonlin-

earity \( \psi \) simplifies the circuit realization of the controller. One

simple analog circuit in which the nonlinearity (3) is divided into

several piecewise sections with each section being realized by

two resistors and a diode is shown in Fig. 3(a) [16]. Thus, even

large FLC rule tables that need more granularity can be realized

with power converters often calls for the use of a digital pro-

cessor and associated interface circuitry [2], [3]. On the con-

trary, the implementation of NLFC using the analog circuit in
Fig. 4. Preprocessing circuit. (a) Realization. (b) Mapping.

Fig. 5. Membership functions. (a) Asymmetrical. (b) Symmetrical. (c) Mapping.

Fig. 3 uses opamps, diodes, and resistors. Besides simplicity, this circuit is also inexpensive when compared to the digital implementation of FLC.

Digital implementations suffer from time delays due to analog-to-digital conversion (ADC) process. For instance, the inexpensive digital implementation in [3] has an ADC delay of about 36 μs. The implementation of fuzzy algorithm also involves time-consuming division operation. These time delays limit the overall closed-loop bandwidth and, hence, the dynamics. In addition, an upper limit on the switching frequency will be imposed if a digital pulsewidth modulation (PWM) module is used. For instance, in [3], the switching frequency is limited to 31.373 kHz by the PWM module. In contrast, the gain–bandwidth product of the opamps used in analog implementation of NLFC in Fig. 3(a) is of the order of several megahertz. Hence, closed-loop bandwidths up to several tens of kilohertz are possible using the circuit in Fig. 3(a). The switching frequency is also not limited by the NLFC. This fact is demonstrated in Section V, where the NLFC is implemented by an opamp (CA3140) having a gain–bandwidth product of 4.5 MHz for a dc–dc boost converter switching at 50 kHz.

E. Handling Asymmetric Input Membership Functions

In the case of asymmetric triangular input sets [5], as in Fig. 5(a), preprocessing of inputs may be needed prior to processing using (2) and (3). This can be explained with the help of an example. At a normalized value of input \( x = 0.5 \), rules related to PM alone are fired in the FLC in Fig. 5(a). On the other hand, rules related to both PS and PM are fired in the FLC with symmetrical input sets for \( x = 0.5 \) [Fig. 5(b)]. This will result in a large error in the defuzzified value, especially when the vertices of the asymmetrical sets are far apart. The error in such cases can be reduced if the set of vertices \((-1, -0.5, -0.2, 0, 0.2, 0.5, 1)\) of the asymmetrical sets are mapped to those \((-0.75, -0.25, 0, 0.25, 0.5, 0.75)\) in the symmetrical sets [refer Fig. 5(c)]. This preprocessing, although not essential in most cases, if unavoidable, may be realized, with an inversion, using the circuit in Fig. 4 [16]. Here, only the positive half of the mapping is shown. It may be noted that, if all of the inputs of an FLC have similar asymmetric membership functions, the preprocessing circuit may be avoided. An example for this will be given in Section IV.

To summarize, an FLC and its simplified form NLFC are virtually interchangeable under the following conditions.

- Input membership functions are symmetric/asymmetric triangular with 50% overlap. Preprocessing circuit may be needed in the case of asymmetric input sets.
- Output membership functions are symmetric/asymmetric triangular with 50% overlap (Mamdani-type FLCs) or singletons (Sugeno-type FLCs).
- The rule table has a Toeplitz or near-Toeplitz structure.

With FLCs satisfying the above three conditions, there will be a closer match of the outputs of FLC and NLFC for the inputs at which rules are defined in the FLC rule table. The overall
rule surfaces of FLC and NLFC will be closer with the degree of
closeness depending upon the rule table’s nearness to the
Toeplitz structure, granularity, fuzzy operators (e.g., AND or OR),
and defuzzification strategies (e.g., centroid and center of sums)
employed. As most of the FLCs implemented with power
converters [1]–[14] satisfy the above three conditions, the substitu-
tion of such an FLC with an NLFC in power converter control
applications is solely investigated in this paper.

F. Verification of Equivalence Between NLFC and FLC

To demonstrate the simplicity of NLFC and its near similarity
to the two-input FLC having a Toeplitz rule table, the Man-
dani-type FLC implemented to control a dc–dc boost converter
in [3] is considered. Table I represents rule table with inputs $x_1$ and
$x_2$ replaced by output voltage error $e$ and change-in-error $ce$.
The input and output membership functions are symmetrical
and are similar to that represented in Fig. 5(b) upon normalization.
Hence, preprocessing gains are not needed in the NLFC
realized. The processed input $d$ (2) of the NLFC may be veri-
fi ed to be the addition of $e$ and $ce$ inputs ($\lambda = 1$). The nonlinear
function mapping $\psi$ (positive-half alone) is shown in Fig. 6(a).
Up to $|d| = 0.5$, the output $r$ follows the input. Due to trape-
zoidal end-sets in the output set, the output $r$ is limited to $\pm 0.8$
(when PL or NL alone is fired). The presence of trapezoidal sets
and saturation have been taken into account by a change in the
slope of $\psi$ beyond $|d| = 0.5$ and the saturation of output $r$ at
$\pm 0.8$ for $|d| > 0.75$. Fig. 6(c) shows the simulated outputs of
FLC and NLFC when excited with inputs [Fig. 6(b)] covering the
$e$–$ce$ plane. By and large, the difference between the two
outputs is negligible, thereby suggesting NLFC as a simple and
cost-effective alternative to the two-input FLC.

III. DESIGN OF A CLASS OF NLFC CONTROLLERS

In this section, the NLFC concept is applied to a large class
of FLCs known as PI-FLCs [10] that are widely used in power
converter control applications. PI-FLCs are FLCs in which the
inputs to the controller are the error $e$ and change-in-error $ce$
of the plant’s output (state) variable. The simplified form of the
PI-FLC, when applying the NLFC concept, yields the nonlinear
PI controller (NPIC), which is introduced in this section. A dis-
cussion on the converter’s dynamic response enhancement fol-

For a PI-FLC, the inputs are given by

$$x_1 = e, \quad x_2 = ce.$$  \hspace{1cm} (4)

The above inputs are fed to the FLC block to compute the
incremental control action $r$, which is further integrated to get
the actual control input to the plant. This integration involved in
postprocessing imparts the name PI-FLC to the controller.

Fig. 7(a) shows the overall schematic of an NLFC with inputs
$x_1$ and $x_2$ and preprocessing circuit gains represented by func-
tions $\Phi_1$ and $\Phi_2$. From this, the NPIC structure has been derived
as shown inside the dotted block in Fig. 7(b). The “filter” block
is used to filter the switching noise of the converter. The pro-
cessed input $d$ in NPIC [Fig. 7(b)] is obtained using

$$d = \frac{\Phi_2(ce) + \lambda \Phi_1(e)}{\sqrt{1 + \lambda^2}}$$  \hspace{1cm} (5)

which in turn is derived from (2) and fed to the nonlinearity $\psi$.

The output $r$ of $\psi$ is multiplied by a gain $m$ and then in-
te grated to get the actual plant control input $D$.

This NPIC in Fig. 7(b) is equivalent to a linear-PI controller,
when the nonlinearity $\psi$ and preprocessing functions $\Phi_1(e)$ and
$\Phi_2(ce)$ are replaced by simple gains. To show this, let us con-
sider a PI controller given by

$$T(s) = \frac{D(s)}{e(s)} = K_1 \cdot \frac{\frac{s}{K_2} + 1}{s} \Rightarrow D(s) = \left(\frac{s \cdot e(s)}{K_2} + e(s)\right) \cdot \frac{K_1}{s}.$$  \hspace{1cm} (6)
The first term in (6) represents the addition of error \( e \) and its derivative (change-in-error \( \alpha e \)) with a gain. The system schematic with PI controller in Fig. 7(c) has been drawn using (6). The similarity between NPIC [Fig. 7(b)] and PI controller [Fig. 7(c)] may be seen. However, it must be noticed that the NPIC has additional nonlinearities that may be tuned appropriately to achieve superior large-signal dynamic performance of the converter over that offered by PI controller.

To achieve a good small-signal transient performance (i.e., for small values of \( d \)) similar to that obtained with a PI controller, the parameters of NPIC obtained upon replacing the nonlinearity \( \psi \) and the preprocessing functions \( \Phi_1(e) \) and \( \Phi_2(\alpha e) \) by unity gains (under the conditions defined in Section II-E) may be matched with those of the PI controller. The relation between error \( e(s) \) and duty ratio \( D(s) \) of NPIC [Fig. 7(b)] under these conditions can be written as

\[
T_{npic}(s) = \frac{D(s)}{e(s)} = \frac{s + \lambda}{\sqrt{1 + \lambda^2}} \frac{m}{s} \Rightarrow D(s) = \left( \frac{s e(s)}{\sqrt{1 + \lambda^2}} + \frac{\lambda e(s)}{\sqrt{1 + \lambda^2}} \right) \frac{m}{s}, \tag{7}
\]

where \( T_{npic}(s) \) is the transfer function from \( e(s) \) to \( D(s) \). The term \( \lambda \) in (7) is the corner frequency of the controller and is generally much greater than 1 rad/s in the case of a switching converter. As a result, the term \( (1 + \lambda^2) \) can be approximated to \( \lambda^2 \). Thus, the parameters of NPIC to achieve good small-signal transient response can be written from (6) and (7) by inspection

\[
\lambda = K_2 \quad m = K_1. \tag{8}
\]

For higher values of input \( d \), i.e., for large disturbances, the equivalent gain of \( \psi \) is set high, so that the plant control input \( D \) changes at a rate faster than that obtained with a linear-PI controller resulting in faster response. Thus, while the NPIC offers matching small-signal performance similar to a PI controller, the large-signal performance offered by it is much better than that obtained with the PI controller. Thus, the proposed NPIC approach, besides resulting in simple implementation, also leads to better insights into the design process.

It may be noted that, in the case of NPICs in which preprocessing circuits \( \Phi_1(e) \) and \( \Phi_2(\alpha e) \) are inevitable, a more detailed model of the controller may be needed for performance enhancement. Besides, at an operating point different from the design operating point, the NPIC (and the original PI-FLC) does not guarantee a good small-signal transient response. This is similar to the case of the linear-PI-based control scheme. Adaptive tuning [10], which is not the focus of this paper, may be needed in such a case.

**IV. VALIDATION OF REPLACEMENT OF THE PI-FLC BY AN NPIC**

In this section, an NPIC for a dc–dc boost power converter is designed. Following this, a Sugeno-type PI-FLC equivalent to this NPIC is derived. Simulation results validating the replacement of PI-FLC by NPIC are presented and discussed.

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**A. System and Controller Description**

Fig. 8(a) shows a dc–dc boost power converter that steps up a dc voltage of low magnitude to one having a higher magnitude, depending on the duty ratio \( D \) of the switch \( S \). The converter considered has a nominal input voltage \( (V_i) \) of 15 V, rated output voltage \( (V_o) \) of 25 V, rated output power of 50 W, and a switching frequency of 50 kHz. The filter elements considered are \( L = 267 \mu \text{H} \) and \( C = 540 \mu \text{F} \).

A linear-PI controller that ensures good small-signal transient performance of the converter at \( V_i = 15 \text{ V} \) and \( R = 33 \Omega \) has been designed

\[
T_c(s) = 3.4 \cdot \frac{s + 1000}{s}, \tag{9}
\]

through MATLAB-SIMULINK [17] simulations. Parasitic elements of the converter that include parasitic resistance of \( L = 0.2 \Omega \), equivalent series resistance (ESR) of \( C = 0.15 \Omega \), on resistance of \( r_s' = 0.115 \Omega \), and forward voltage drop of diode \( D_1 = 0.8 \text{ V} \) have also been considered in the design.

The parameters of NPIC/PI-FLC that ensures an identical small-signal behavior of the converter is derived from the above PI controller using (8). They are as follows:

\[
\lambda = K_2 = 1000 \quad m = K_1 = 3.4. \tag{10}
\]

The cut-off frequency of filter in Fig. 7(b) is set at 10 kHz. The differentiator block is approximated by a transfer function with a zero at the origin and a pole at 3500 Hz.

The range of input \( d \) of NPIC, beyond which the nonlinearity \( \psi \) will have a gain higher than unity, has been decided by small input voltage perturbations on both the system schematics, i.e., with PI controller [Fig. 7(c)] and with NPIC [Fig. 7(b)] using MATLAB-SIMULINK. Matching small-signal performances with both NPIC and PI controller were obtained when the nonlinearity \( \psi \) was set to have a unity gain for \( |d| \leq 0.8 \text{ units} \).
Beyond $|d| = 0.8$, the nonlinearity $\psi$ has been tuned through simulations on the NPIC-based boost converter model [see Fig. 7(b)] using input voltage perturbations of varying magnitudes with an aim to get good large-signal response.

In the actual implementation, as the gain of $\psi$ is high at higher values of input $d$, many times, opamp saturation was found to hinder the realization of the desired nonlinearity. To avoid this, the gain of nonlinearity has been reduced by a factor ($\approx 1/4.44$) and appropriately compensated for by an increase in the output gain $m$, which is realized in the integrator stage. The corrected value of $m$ is given by

$$m = 4.44 \times 3.4 \approx 15.1.$$  \hspace{1cm} (11)

The nonlinear function ($\psi$) mapping from $d$ to $r$ is shown in Fig. 8(b). Here, it may be noticed that the gain at origin is no longer unity but is reduced to 0.225 ($\approx 1/4.44$).

B. Showing the Equivalence of PI-FLC and NPIC

To derive a PI-FLC approximately equivalent to the designed NPIC, the range of NPIC’s input $d$ ($-6.325$ to +6.325) is divided into five sections ($-6.325$ to $-1.6$, $-1.6$ to $-0.8$, $-0.8$ to 0.8, 0.8 to 1.6, and 1.6 to 6.325). The inputs to the PI-FLC are the processed error $e_{p}$ ($\approx e$) and processed change-in-error $ce_{p}$ ($= ce/(1 + \lambda^2)^{1/2}$, $\lambda = 100$). The range of each of the inputs $e_{p}$ and $ce_{p}$ is limited to $\pm 6.325$ and is divided into seven membership functions as shown in Fig. 9.

Table III is the generated rule table. To obtain the elements of this rule table, the values of $d (= e_{p} + ce_{p})$ corresponding to the vertices ($-6.325$, $-1.6$, $-0.8$, 0, 0.8, 1.6, 6.325) on the inputs $e_{p}$ and $ce_{p}$, for which rules are defined on the table are found. Then the output singleton value corresponding to this $d$ is obtained from the nonlinearity $\psi$ of NPIC. It must be noted that although the rule table (Table III) seems to have a non-Topelitz structure, it may be established to have a Topelitz structure upon increasing the granularity of the input sets and rule table. It must also be noted that, as both the inputs $e_{p}$ and $ce_{p}$ have similar asymmetry in their membership functions, additional preprocessing circuits have been avoided as mentioned in Section II-E.

A plot of rule surfaces of NPIC and PI-FLC (not shown here due to space limitations) showed a reasonably close match of the two surfaces. To demonstrate the near-identical control performance of the NPIC and PI-FLC, simulations were carried out on the boost converter for random changes in reference voltage, load resistance, and input voltage. Fig. 10 shows the corresponding output voltage transient response. The responses with both of the controllers are virtually indistinguishable. Thus, it is clearly established that the NPIC is a good, simple, and fast approximation of a PI-FLC.

V. SIMULATION AND EXPERIMENTAL RESULTS

The nonlinearity $\psi$ of NPIC has been realized using the circuit in Fig. 3(a). The components values are as follows:

- $R_{1} = 12 \, k\Omega$
- $R_{2} = 2.7 \, k\Omega$
- $R_{3} = R'_{3} = 1.8 \, k\Omega$
- $R_{4} = R'_{4} = 36 \, k\Omega$
- $R_{5} = R'_{5} = 2.2 \, k\Omega$
- $R_{6} = R'_{6} = 22 \, k\Omega$

The opamp used in the realization is CA3140E. Fig. 11(a) and (b) shows $\psi$ (inverted) of the NPIC. Due to forward voltage drops of diodes and the tolerance of the resistors, the break points are not sharp and are slightly different from the designed values. The positive and negative saturation levels of $\psi$ are slightly different due to opamp characteristics.

Computer simulations and experiments were performed on the boost converter fitted with both the NPIC and linear-PI controller for small-signal disturbances occurring in load resistance $R_{L}$, reference voltage $V_{ref}$, and input voltage $V_{in}$. It was found, as expected, that the transient response of the converter with the two controllers were nearly identical. This clearly shows that...
NPIC and hence PI-FLCs perform similar to a PI controller for small-signal perturbations.

NPIC is expected to outperform a linear-PI controller for large-signal transient disturbances. Figs. 12–15 compare the large-signal dynamic responses of boost converters with NPIC and PI controllers. Step disturbances in load resistance $R$, reference voltage $V_{\text{ref}}$, and input voltage $V_i$ have been considered in these simulation/experimental results.

Fig. 12(a) and (b) shows the experimental response for a large-step load resistance change. The settling time with NPIC is about 7 ms while that with PI controller is about 15 ms.
results demonstrating the superior performance of NPIC (and hence PI-FLC) over a linear-PI controller have been presented.

REFERENCES

Ramesh Oruganti (SM’01) received the B.Tech. and M.Tech. degrees from the Indian Institute of Technology, Madras, and the Ph.D. degree from the Virginia Polytechnic Institute and State University, Blacksburg, in 1987.

After receiving his doctoral degree, he was with the Corporate R&D Division, General Electric Company, Schenectady, NY, working on advanced power converter systems. Since 1989, he has been with the Electrical and Computer Engineering Department, National University of Singapore, Singapore, where he is currently an Associate Professor and the Director of Centre for Power Electronics. He is active in research on several areas of power electronics, including soft-switched power converters, converter systems for power quality applications, modeling and control of power converters, and AI applications in the control of power converters. He holds a patent on dc–dc converters.

Dr. Oruganti was the recipient of two prize paper awards.

Dipti Srinivasan (SM’00) received the M.Eng and Ph.D. degrees in electrical engineering from the National University of Singapore (NUS), Singapore, in 1991 and 1994, respectively.

She was with the Computer Science Division, University of California, Berkeley, as a Postdoctoral Researcher from 1994 to 1995. In June 1995, she joined the faculty of the Electrical and Computer Engineering Department, NUS, where she is an Assistant Professor. Her research interests are in the application of soft computing techniques in power system operation, economics, and control.