The implementation methodology of the real effects in a NOI nanostructure, aided by simulation and modelling

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Abstract

The SOI transistors permanently offer new candidates as nanodevices. The nothing on insulator NOI transistor was recently derived from the nano SOI–MOSFET family. Their output characteristics were theoretical modelled with an exponential law, validated by simulations. The transfer characteristics presented sometimes increasing and others times decreasing monotony. This phenomenon was put directly into a relationship with the gate tunnelling breakdown. This paper has three final targets: the breakdown limitation through the back-gate terminal, the real effects including in the NOI transistor architecture – like interface charges or metal-semiconductor work function and quantum effects corrections in simulations, in order to produce a better correlation between simulations and a real behaviour. These simulations represent a milestone in the NOI nanotransistor manufacturing, establishing some parameters that link the device to the real work regime.

1. Introduction

The modelling and simulations of the electronic devices have a great impact onto the micro and nano electronics technology: to conceive new devices [1], to optimize some work regimes [2], to comprehend some physics phenomena [3] or real behaviour [4,5], to simulate a failure mechanism [6], to construct a virtual lab to test a device [7,8], or to efficiently design and produce a device with minimum financial and time spending [9]. The analytical models and the devices simulations, besides to the enormous help offered to the designers and technologists engineers, fill a gap that nowadays still occurs between the produced nanostructures and the phenomena inside them [10–12].

The silicon on insulator (SOI) transistors were first time developed as radiation-hardened devices due to the oxide support [13]. Lately, a lot of SOI devices were developed for others purposes: high temperature devices without junctions, microsensors [14], low power devices [15], special cMOS transistors [16]. Different materials on insulator were also intensively studied in the last decade. Some authors propose the lateral growth of Ge on silicon oxide layers, from nanoscale silicon seed. The germanium growth starts selectively from the silicon seed lines and proceeds by wetting the SiO2 layer, providing monocrystalline films, free of bulk defects [17]. Others authors used silicon carbide and diamond to improve the static characteristics [18,19]. Also alternative biomaterials to the organic semiconductors as pentacene [20] were searched in order to allow a non-linear electrical conduction. Among the investigated Biomaterials On Insulator, which offer a field effect transistor behaviour, were studied some neuro-hormonal aq. solutions – inspired from their conduction with threshold at the synapses level [21,22], some lipophilic steroids with a good non-linearity of the transfer characteristics: sub-nA currents under 5 V and tens of micro-amps over the prior threshold voltage [23].
The SOI family permanently offers news candidates as nanodevices, due to the integration of the active component into the ultra-thin Si membrane. In this scope, the classical SOI–MOSFET was modified to offer a higher current sensitivity in a given value vicinity for the gate voltage [24]; then the SOI film was thinned and etched in the channel region in order to provide two conduction ways: vacuum tunnelling [25] and MOS inversion channel [26]. This last SOI nanostructure, presented in Fig. 1, was the starting point for the NOI transistor concept. In 2008 an application was proposed for the previous SOI nanodevice with a vacuum cavity and with sub-10 nm film thickness; the single electron transistor SET implementation due to the shape of the $I_D-V_{GS}$ characteristics with a maximum, like is the SET demand [27,28]. These nanostructures can be experimentally produced because the nowadays upper semiconductor layer can reaches tens of nano-meters, grace to the SIMOX or Unibound technology [13,29,30].

The NOI transistor is a novel candidate in the nano-devices arena that alternatively combines the “Silicon” with “Nothing” as materials on insulator. From this point of view it has arisen as a natural downscaling of the semiconductor channel region of the prior SOI–MOSFET with a cavity [31] and has received the acronym NOI that means nothing on insulator, in a similar manner as was defined the SON transistor as silicon on nothing, derived inside the SOI family too [32]. The first studied NOI device had the source and drain Si–n$^+$ regions with sizes: $x_{n^+} = 3$ nm, $y_{n^+} = 7$ nm, $d = 2, \ldots, 5$ nm and substrate oxide thickness $y_{ox} = 10$ nm. The first simulations assumed an ideal structure, without charged interfaces and avoiding quantum corrections. However, those simulations revealed a non-linear conduction between source and drain, gate assisted: for $V_{DS} = +8$ V the drain current reached 40 pA if $V_G = +0.01$ V and 180 pA if $V_G = +1$ V, when $d = 4$ nm [31]. The simulations proved a strong dependence of the operating voltages versus the distance $d$: for $V_{DS} = 1$ V the drain current $I_D$ reaches 0.02 pA if $d = 1.5$ nm, or 50 nA if $d = 0.5$ nm. The results are expectable due to the exponential law $I_D \sim d$ [31]. The physical explanation comes from the tunnel effect that must occur on longitudinal direction in order to allow the source–drain current flow.

Among the advantages of the proposed NOI device can be mentioned: simplified SOI technology without additional $p$ zone for the channel region besides existent n$^+$ – islands, non-necessary a vacuum technology due to 1–2 air molecules in cavity [25], higher integration density due to the nano-metric sizes, radiation immunity due to the SOI architecture [13].

The disadvantages of this device consist in: difficulties in manufacturing due to its small sizes – but not more expensive than a classical SOI nanotechnology, relatively high operation voltages due to the insulators breakdown work principle and an additional failure mechanism toward substrate modelled and optimizes in this paper.

The NOI's distinct and own static characteristics make it suitable for others applications than the standard nano-MOSFETs. The same situation occurred with the SET nanotransistor, which presents at typical characteristics due to the Coulomb blockade and was suitable for oscillators, SEM memories [33]. Some possible applications of the NOI nanodevice could be in the nanoelectronics manufacturing [34], 3-D nanoelectronics integration [31], vacuum devices for spatial applications [35], or devices for biomedical applications [36,37], hardened devices for in vivo investigations inside tumoral tissues frequently invaded with nuclear nanoparticles [38,39].

2. The NOI structure presentation and links to nanofabrications

The NOI transistor architecture was inspired from a real sub-10 nm undulated poly-silicon on insulator, Fig. 2. A study about the fabrication technique of a thin undulated poly-silicon film deposited onto an insulator material is detailed presented by Badila [40]. The solution was by Secco etching that preferentially etches the boundaries of the grains, producing undulated poly-silicon layer with maximum 7 nm and minimum 3 nm thickness, Fig. 2. The active device was placed on a 50 nm oxide, and biased like a pseudo – MOS transistor via substrate contact [41]. That nanodevice was a bridge among pseudo-MOS, SOI–MOSFETs and few electron transistors, borrowing some features from all of the prior transistors [42]. This relationship is obviously in the obtained transfer characteristics when the gate voltage was increased from 0 V to 15 V maintaining $V_{DS} = +500$ mV and the drain current varied from 0.1 nA to 8 nA [43]. An optimization study made by modelling and simulation to this thin film nanotransistor with polysilicon grains improves the transfer characteristics, considering as real effect the dispersion of the trap-state energy [44].

![Fig. 1. The SOI–MOSFET with a cavity in the channel region.](image-url)
The above technological method could be applied to manufacture the NOI nanostructure, extending the time etching till the Si valleys touch the oxide. In others circumstances, the "Nothing" space resulted by the etching of a silicon membrane, in the silicon on nothing technology [45].

The first adjustment brought to the undulated structure was to preserve only two silicon nano-islands with rectangle shape and 7 nm height. The film thickness was decreased into the channel region from \( y_p = 3 \, \text{nm} \) to 1 nm, then to 0.3 nm, while the source and drain \( n^+ \)-type films were preserved at a constant 7 nm thickness [25]. This special "U" shape SOI–MOSFET is the starting point for the NOI transistor.

As in the case of experimental sub-10 nm undulated poly-silicon film on insulator, the "U" shape SOI–MOSFET revealed a new shape of the \( I_D–V_{DS} \) characteristics [46]. In this way, the simulations were in agreement with the experiments that prove the current confinement through a thinner film [43,46]. This SOI–MOSFET transistor, with a thinner film in the channel region presents monotonically increasing current if the Si thickness is higher than 10 nm or a characteristic with minimum if the Si thickness decreases under 7 nm [46]. Fig. 3a presents two main currents through a cross section of the "U" shape SOI–MOEFET: the \( I_{\text{MOS}} \) current that prevails for a thicker channel region and \( I_{\text{tunnel}} \) that occurs in vacuum and is responsible for the curve \( I_D–V_{DS} \) with a minimum.

Completely removing the semiconductor film between source and drain, a NOI – nothing on insulator structure resulted, Fig. 3b. As is shown in this last figure, the "Nothing" region represents the NOI transistor body, or the main physical place where the source–drain conduction occurs. Due to the gate bias influence on this current, the NOI structure belongs to the field effect transistors class.

The substrate is acting as a back-gate, simply named Gate here \( G \), which controls the source–drain current. This is possible in a SOI configuration that usually has 2 gates: front-gate and back-gate [47]. A recent study demonstrated a better control of the ultrathin SOI devices (~8-nm thickness) if the back-gate is used, due to the improvement in the short channel control, equivalent with 10% higher drive current, 10% shorter gate lengths [48].

As a last observation, can be mentioned that a mechanical boring of the underneath oxide film is not possible, because the standard manufacturing process starts on standard wafers, thick enough (hundreds of microns) to ensure the mechanical integrity of the nanodevice.

**Fig. 2.** A manufactured SOI nanotransistor with maximum 7 nm.

**Fig. 3.** (a) The SOI–MOSFET, with a thinner p-film in the transistor body, \( y_p < y_{nr} \); (b) the NOI nanotransistor with \( y_p = 0 \), and a conceptual representation of the tunnel current.
3. The output characteristics

As a short history, can be mentioned that in these kinds of SOI nanodevices, with thicker p-type film ($y_p > 50$ nm), the MOS current prevails even in diamond on insulator structures and the classical shape with saturation of the $I_D - V_{DS}$ characteristics occurs [49]. In thinner SOI devices (e.g. for $y_p \leq 1$ nm, Fig. 1) the tunnel current prevails. The $I_D - V_{DS}$ curve presents a minimum, after ATLAS running at $V_{GS} = +3$ V, due to the superposition of the MOS - type current and tunnel current, Fig. 4a. All the time the source was grounded, $V_S = 0$ V. For these “U” shape transistors, with lower currents variation, the linear scale is more suitable for representation.

Fig. 4 presents the $I_D - V_{DS}$ curves evolution for the nanotransistor with cavity, from SOI to NOI that means for $y_p = 1$ nm, $y_p = 0.3$ nm in Fig. 4a, to $y_p = 0$ nm in Fig. 4b. In the NOI case, the currents exponentially increase and a logarithmic scale is more suggestive.

When the device becomes NOI that means $y_p = 0$ nm, the current flow on the longitudinal direction is ensured by the drain–source voltage, with a specific tunnelling phenomenon through a triangle potential barrier [50]:

$$I_D(E_{ds}) = \frac{A}{\sqrt{E_b}} \cdot \frac{E_{ds}}{d} \cdot \exp \left( -\frac{B \cdot E_{ds}^{3/2}}{E_{ds}} \right)$$

where $E_b = \kappa_{\text{semic}} - \kappa_{\text{vacuum}}$ is the height of the triangle barrier potential from semiconductor to vacuum, $\kappa_{\text{semic}}$ is the electrons affinity in semiconductor and $\kappa_{\text{vacuum}}$ is the electron affinity in vacuum, $E_{ds} = -\text{grad}V_{DS}$ is the electric field in vacuum induced by the $V_{DS}$ voltage, $I_D$ is the drain tunnel current and $A$, $B$ are material parameters [50]. The dependence $I_D(E_{ds})$ from the expression (1) was validated by simulations. In the narrow vacuum cavity, a linear dependence of the electric field can be assumed: $E_{ds} = V_{DS}/d$, where $d$ is the vacuum distance presented in Fig. 1. The first order derivative $I_D'(V_{DS})$ can be computed from Eq. (1):

$$I_D'(V_{DS}) = \frac{A}{\sqrt{E_b}} \cdot \frac{V_{DS}}{d} \cdot \frac{d}{V_{DS}} \cdot \left( 2 + \frac{B \cdot E_{ds}^{3/2}}{V_{DS}} \right)$$

Because $I_D'(V_{DS}) > 0$ for $V_{DS} > 0$, accordingly with the analytical model (1), results that the tunnel current monotonically increases with the drain–source voltage. The simulations are in agreement with the theoretical point of view regarding the function (1) and a similar monotony results for the simulated $I_D - V_{DS}$ output characteristics too, Fig. 4b.

In order to detect the field effect transistor, a dependence of the drain current versus the gate voltage must be emphasised. A first step is made in Fig. 5, where two distinct gate voltages give two distinct curves of currents. Besides is shown the vectors of the total current that penetrate the vacuum cavity for $V_{GS} = +3$ V, Fig. 6.

4. The transfer characteristics

The transfer characteristics were studied, in order to demonstrate the NOI nanotransistor affiliation to the field effect transistors class. The gate terminal is the back-gate of a traditional SOI transistor. As work principle, the $V_{GS}$ voltage variation must modulate the electrons concentration in the Si–$n^+$ islands. This is the key phenomenon that makes possible the gate control on the drain current only in semiconductor source/drain islands. In metals a gradient of the carriers is not possible. Increasing the gate voltage from 0 V to 6, ..8 V, within the anticipation of the metal-semiconductor work function, the carrier concentration is strongly modulated in the semiconductor islands placed on insulator [51]. The consequence is a

![Fig. 4.](image-url)
crowding of the current vectors near the insulator surface and a rarefaction of them through the top, accordingly with the carriers distributions, as is suggestive presented in Fig. 6. Since to be focused on this effect, first time the vacuum/oxide, silicon/vacuum interfaces were considered ideals and free of charges [31]. Fig. 7a presents the first set of output characteristics. The $I_D-V_{DS}$ simulated curves are inconsistent: at low $V_{DS}$ (e.g. for $V_{DS} = +0.3$ V) the drain current increases with the $V_{GS}$ rising and at high $V_{DS}$ (e.g. for $V_{DS} = +3$ V) the drain current decreases with the $V_{GS}$ rising. The explanation comes from simulations that surprised some quite distinct currents: $I_D$, $I_S$ and $I_G$: $I_G/25/C_0 I_S$ and $I_D$? 0 for $V_{GS} > 4$ V, where the index S, D, G represents source, drain and gate, Fig. 7b. The simulator finds out a negative source current that means its sense changing. A significant gate current $I_G = 0.003$ pA/25/C_29 I_D = 0.00004 pA when $V_{DS} = 3$ V, $V_{GS} = 4$ V, is the best proof for the oxide breakdown. These simulations demonstrated the parasitic tunnelling of the oxide support with 10nm thickness, besides to the useful vacuum cavity tunnelling. This gate leakage current was interpreted as a breakdown phenomenon in the NOI structure with unrealistic thin buried oxide [52]. This extra-thin oxide (10 nm) was selected only from simulations reasons.

But a real trade-off between the breakdown limitation and the gate-voltage control on the drain current is a target of this paper. In this communications the structure was changed so that the gate leakage current be minimised, the real interfaces properties and the updated doping concentration in Si–n+-type islands be introduced.

On the other hand, our NOI device is free from the channel pinch-off at relatively high operation voltages [53], because a saturation of characteristics did not occur in any simulations. A solution to decrease the gate and drain operation voltages can be to select others materials as insulator, (e.g. high-k, etc), [54]. This scope is performed in this paper, comparatively simulating the silicon on oxide and on sapphire – two suitable materials for SOI technologies.

**Fig. 5.** Simulations of the output characteristics of NOI transistor at two $V_G$ values, represented at linear scale.

**Fig. 6.** The current flow vectors in the simulated NOI structure at $V_G = +3$ V.
5. Updated NOI nanostructure

The previous simulations, from the 3rd and 4th paragraphs, were achieved for a NOI structure with: \( x_n = 3 \) nm, \( y_n = 7 \) nm, \( z_n = 7 \) nm, \( y_p = 0 \) nm, \( y_{ox} = 10 \) nm (notations from Fig. 1), metal-semiconductor work function 0 V and without electric charge in oxide.

A first correction in the present simulations is related to the mesh space on Ox, Oy axis, at 0.3 nm, equal with the inter-atomic distance, in order to numerically solve the Poisson equation from node to node that now signify the atom places, closer to reality.

The second adjustment regards the actual Si islands sizes: \( x_n = 4 \) nm, \( y_n = 10 \) nm, \( z_n = 10 \) nm, \( y_p = 0 \) nm, \( d = 3 \) nm. The insulator was first time oxide Fig. 8a and another time sapphire, Fig. 8b.

The old doping concentration \( N_D = 10^{17} \) cm\(^{-3}\) means 0.04 impurities/\( n^+ \) island, so unrealistic. As a third correction, \( N_D \) was increased to \( 2 \times 10^{21} \) cm\(^{-3}\), that means 800 impurities/\( n^+ \) island volume. If the doping concentration is rising in the \( n^+ \) source and drain islands, a higher electric charge quantity is available for tunnelling. Hence, a sharper gate-control

![Fig. 7](image-url) *(a) The first set of output characteristics; (b) The evolution of the \( I_D-V_{GS} \) characteristics for different \( V_{DS} \), emphasising the \( I_L \) rising, too.*

![Fig. 8](image-url) *(a) The simulated NOI structures with inter-atomic grid distance both in film, vacuum and insulator support: (a) for \( x_n = 3 \) nm, \( y_n = 7 \) nm and oxide support; (b) for \( x_n = 4 \) nm, \( y_n = 10 \) nm and sapphire support.*
on current is expected. Obviously, the $N_D$ selection, as much as possible, is useful to emphasise the field effect of the NOI transistor, but is superior bordered by the Si atoms volume concentration $\sim 10^{22}$ cm$^{-3}$.

A more refined grid in the device body versus the poor mesh previously used, has now a considerable influence on the $I_D$, $I_S$, $I_G$ currents, consisting in a higher accuracy. Even for $I_C = 0.1$ pA that means far away from the breakdown conditions, the source and drain currents are quite distinct now (Fig. 9a): $I_S = 7.2$ nA $> I_D = 0.8$ nA $\gg I_D = 0.0001$ nA from the old case (Fig. 4b), when $V_{DS} = 4$ V, $V_{GS} = 1$ V. The explanation is related to a different concentration of carriers in the drain and source regions with higher sizes, rigorously computed at inter-atomic distance between atoms. Unfortunately, rising the gate voltage at $V_G = 10$ V, the oxide breakdown still occurred. This can be proved from the currents point of view, Fig. 9a, as well as from the carrier’s point of view, Fig. 9b.

From Fig. 9b can be observed that the electrons concentration reaches $n > 2 \times 10^{21}$ cm$^{-3}$ in the source region, while it reaches $n < 5 \times 10^{20}$ cm$^{-3}$ in the drain region. This is an explanation for the lower drain current than the source current in Fig. 9a, which is directly related to the carriers concentration.

6. The breakdown limitation

The premature breakdown at $V_{GS} = 3$, …, 4 V is predictable for 10 nm oxide thickness. In the real case, the nanodevice body, composed by few atomic layers, must be placed on a hard support, thick enough to allow the device handling (e.g. a SOI wafer). As a forth correction, a standard SIMOX wafer with 400 nm buried oxide [55], was admitted as support for the NOI device. In this case, the simulated leakage current through the gate is completely avoided, $I_C = 10^{-14}$ A $\ll I_D = 2 \ldots 8$ nA, Fig. 10.

The Atlas simulations have taken into account in the MODEL statement all the parameters that emphasise the oxide breakdown: band to band tunnelling, Fermi distribution, mobility’s models with transversal field dependence by the parameters: BBT, Fermi, fldmob. Fig. 10 presents all the currents through the NOI nanotransistor terminals, when $V_S = 0$ V, $V_D = 4$ V, $V_G = 0 \ldots 5$ V, with negligible $I_C$ current that demonstrates no breakdown through the gate electrode. The anti-symmetry of the $I_D$ and $I_S$ currents here, demonstrated that they are equals in modulus, in agreement with no leakage toward substrate or gate terminal.

On the other hand, the 400 nm oxide thickness is not compatible with the “nano” concept. Additionally, the transfer characteristic is strongly alleviated, with a weak variation for $0 < V_C < 4$ V: the drain current ranges only from 1.9 nA to 1.9015 nA. These reasons let us to try a thinner oxide substrate. So, a thinner oxide layer was simulated and the gate current was recorded for $0 V < V_G < 5$ V. A first limit of the oxide thickness was 200 nm, when an incipient leakage gate current occurs, but it is far away from the breakdown conditions. In this last situation the gate current increases from $10^{-24}$ A at $V_{GS} \approx 2$ V to $4 \times 10^{-12}$ A at 5 V and is still negligible in respect with the source current that is about $5 \times 10^{-9}$ A.

**Fig. 9.** (a) The influence of refined grid on the modulus $I_D$, $I_S$, $I_G$ currents versus $V_{DS}$ at $V_{GS} = 1$ V; (b) Electrons concentration in the source and drain region at $V_{DS} = 4$ V and $V_{GS} = 10$ V with breakdown emphasising ($n = 2.5 \times 10^{21}$ cm$^{-3}$ near Vacuum cavity and $n = 2.4 \times 10^{21}$ cm$^{-3}$ near oxide substrate).
On the other hand, as a fifth optimization, two materials were simulated for the insulator support: oxide and sapphire. The simulated structure on sapphire is available in the Fig. 8b. At \( V_D = 4 \text{ V} \), \( V_G = 4 \text{ V} \), \( V_S = 0 \text{ V} \) results the currents \( I_D = 7.6 \text{ nA} \) for oxide and \( 33 \text{ nA} \) for sapphire, both with ideal interfaces. Hence, the sapphire provides a higher signal at the same stimulus. Regarding the breakdown performances, the results are reverse: \( I_G = 2 \text{ pA} \) for oxide and \( 93 \text{ pA} \) for sapphire at the same voltages. For this reason, the sapphire offer 4 times better field effect of the transistor, but 40 times poorer quality in the gate leakage current. Therefore, the sapphire was ignored in the next paragraph.

7. The interfaces effects accounting

In this paragraph, the NOI structure with \( x_{n+} = 4 \text{ nm}, \ y_{n+} = 10 \text{ nm}, \ z_{n+} = 10 \text{ nm}, \ y_p = 0 \text{ nm}, \ d = 3 \text{ nm}, \ N_D = 2 \times 10^{21} \text{ cm}^{-3} \) and 200 nm oxide was simulated, taking into account real aspects, as a sixth correction: (1) the interface charge Si/oxide is \( Q_f = 5 \times 10^{10} \text{ e/cm}^2 \), (2) an n-type poly-Si as source and drain materials are defined, with the work-function \( \Phi_{MS} = -0.55 \text{ V} \) accordingly with Atlas library [56].

At \( V_D = 4 \text{ V} \), \( V_G = 4 \text{ V} \) results \( I_D = 6.1 \text{ nA} \) for an ideal oxide and \( I_D \) becomes 5146 nA for the real oxide with the previous \( Q_f \) and \( \Phi_{MS} \) values, proving the electrons crowding in the bottom of \( n^+ \)-island, due to the positive interface charge. Besides to the drain current shift, these real effects change the \( I_D-V_{DS} \) shape as is comparatively shown in Fig. 11a and b. Due to the \( n^+ \) doping, just the electron currents, \( I_{SD,n} \), as the main component of the majorities carriers were represented. In the ideal structure, the source electrons current, \( I_{S,n} \), becomes higher than the drain electrons current, \( I_{D,n} \), for \( V_{DS} > 2 \text{ V} \), due to the tunnel effect onset, Fig. 11a. This inequality is maintained in the real structure, too. It is obviously that not all the emitted electrons, from the \( n^+ \)-source region, cross the vacuum and arrives to drain. Part of them is taken back to source and another part flows toward the insulator support. On the other hand, the shapes of the total currents \( I_{D,tot}, I_{S,tot} \) are modified in the real case when \( Q_f \) and \( \Phi_{MS} \neq 0 \), Fig. 11b. The electrons component current increases very fast at \( \approx 5000 \text{ nA} \) for \( V_{DS} = 0.2 \text{ V} \) in the real case because the positive interface charges initially produced an electrons accumulation, hence an enhancement of the electric charge in the \( n^+ \)-source and drain regions. The output characteristics with saturation bring the NOI nanotransistor behaviour in the real case, closer to a classical filed effect transistor. However, only a simulator can reveal a distinction between the total current and the electron current, Fig. 11b. The shape is completely different among these currents. Surely, the total current \( I_{D,tot} \) and \( I_{S,tot} \) for the NOI structure with real interfaces have other order of magnitude due to the \( Q_f \) and \( \Phi_{MS} \) presence. Fig. 11 gives also an example of the distinction between the majority carriers current and total current through a terminal of the NOI device. This difference was also observed in the previous simulations and they prove the huge importance of the minority carrier current that makes the difference: even a concentration about 1...5 holes/island volume, which is a high level of injection, is important at these nano-sizes.

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**Fig. 10.** For 400 nm oxide thickness, the currents \( I_D, I_S = 0 \), but \( I_G = 0 \).
The quantum effects accounting

In deep submicron MOS device, quantum effects have significant effects on the device characteristics, [57]. Also another ultrathin SOI device, with a cross section of 3 times 3 nm² and gate length of 15 nm, was approached by Buran et al., as a quantum device. They compute the transfer characteristics based on a full 3-D real-space self-consistent Poisson–Schrodinger solver, [58]. The method allows to exactly account for characteristics by the mode-mixing.

The effect of the quantum confinement can be taken into account in ATLAS with Schrodinger’s equation solving, with Schro parameter, or simpler with Van Dort model [56]. In this last model, the effect of the quantum confinement is modelled by an effective broadening of the band-gap near surface and is taken into account as the seventh correction in our paper:

\[
\Delta E_g = B \cdot \frac{\beta}{13} \cdot \frac{1}{9} \cdot \frac{\varepsilon_S}{E_T} \cdot \left(\frac{E_T}{4qkT}\right)^{1/3} \cdot E_T^{2/3} \cdot g(y)
\]

where \( \beta = 6.1 \times 10^{-8} \) eV cm, \( E_T \) is the transversal electric field near surface, B.Dort is a user definable adjustment parameter for \( \beta \) corrections, \( T_L \) is the temperature, \( k \) is the Boltzmann constant, \( q \) is the elementary electric charge, \( \varepsilon_S \) is the Silicon dielectric constant, and \( g(y) \) is the distance from surface, given by:

\[
g(y) = \frac{2 \cdot \exp \left(-\left(\frac{y}{\xi_{100}}\right)^2\right)}{1 + \exp \left[-2\left(\frac{y}{\xi_{100}}\right)^2\right]}
\]

Fig. 11. The electron component current for the source and drain currents versus \( V_{DS} \) at \( V_G = 4 \) V in: (a) the ideal structure; (b) the real structure with the same sizes as ideal structure but with \( Q_f = 5 \times 10^{10} \) e/cm² and \( \Phi_{GS} = -0.55 \) V.

8. The quantum effects accounting

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\]

Fig. 12. The simulated transfer characteristics: (a) \( I_D-V_{GS} \) roughly constant for 400 nm oxide thickness; (b) \( I_D-V_{GS} \) with a more obvious variation for 50 nm oxide thickness.
The quantum effects were taken into account in the simulations, including the N.Dort option in the models statement. The previous NOI structure with $N_O = 2 \times 10^{21} \text{ cm}^{-3}$, $x_{\text{n}} = 4 \text{ nm}$, $y_{\text{n}} = 10 \text{ nm}$, $z_{\text{n}} = 10 \text{ nm}$, $y_{\text{p}} = 0 \text{ nm}$, $d = 3 \text{ nm}$ and real interfaces with $Q_0 = 5 \times 10^{10} \text{ e/cm}^2$, $\Phi_{\text{MS}} = -0.55 \text{ V}$, was simulated.

To increase the simulations accuracy in this NOI nanotransistor versus the prior case [31], here also were maintained the Ox, Oy mesh at inter-atomic distance 0.3 nm in the Si film and vacuum. The self-consisting solving of the Poisson and Van Dort equations is possible along nodes, assumed now as atoms. The time simulation considerable increases now. Therefore, the Ox, Oy mesh distance was re-established at 1 nm in the insulator support, where isn’t the device main body, in order to avoid an excess nodes number and to gain in the simulation time domain.

Then the $V_G$ voltage was firstly increased from 0 V to 5 V; secondly the $V_C$ voltage was increased from 0 V to 10 V to observe the transfer characteristic. In order to avoid the gate breakdown, the first oxide thickness was 400 nm. Unfortunately, the gate-control on the drain current is still poor in this case, but the advantage is zero leakage current through the gate terminal (in fact $I_C_{\text{maxim}} = 1 \times 10^{-15} \text{ A}$), Fig. 12a. Therefore, a thinner oxide film was simulated, in correlation with a higher doping concentration $N_O = 4 \times 10^{21} \text{ cm}^{-3}$, to enhance the gate control. The final trade-off between breakdown limitation and gate control on the drain current stopped at 50 nm the oxide thickness and a higher donor impurity concentration in the $n^+$-film. In this way, the optimum was reached in Fig. 12b: a low leakage current $\sim 0.1 \text{ nA}$ through the gate terminal, associated with a steeper variation of the transfer characteristics $I_D-V_{GS}$. It is obviously from Fig. 12 versus Fig. 10 that the quantum effects accounting have affected the gate-control effect on the drain current. The Van Dort model included in simulations suggests a thinner oxide layer, than the classical model, which avoid the breakdown.

9. Conclusion

The paper has presented an evolution of the nothing on insulator (NOI) nanotransistor form the ideal to real structure, highlighting some specific phenomena arising in the device behavior. The paper integrates all these effects, providing a significant progress in the understanding of the NOI transistor itself.

Some corrections are taken into account in order to: bring the simulations closer to the real effects, to avoid the gate breakdown and to reinforce the gate-control on the drain–source current.

A more refined grid on Ox, Oy axis, closer to the interatomic distance, increases the accuracy of the simulated characteristics. Then, the doping concentration was increased from $N_O = 10^{17} \text{ cm}^{-3}$, to $N_O = 2 \times 10^{21} \text{ cm}^{-3}$, then to $N_O = 4 \times 10^{21} \text{ cm}^{-3}$ in the last simulation, in order to increase the current sensitivity at the gate bias. The relationship between current carriers and carriers concentration in the $n^+$ source and drain regions is straight related to the source–drain tunnel phenomenon.

The solution for the oxide breakdown avoiding came from another correction: thicker insulator layer. The investigated thicknesses were in the range 10 nm ... 50 nm ... 200 nm ... 400 nm, when, respectively the ratio $I_{C}/I_{D}$ decreases from: $10^3 \ldots 10^1 \ldots 10^{-3} \ldots 10^{-5}$. For 200 nm oxide thickness and free of charges interfaces resulted: $I_C = 10^{-12} \text{ A} \ll 10^{-9} \text{ A} = I_D$ at $V_{GS} = V_{DS} = 4 \text{ V}$. If the oxide is the more convenient material for the breakdown limitation, the sapphire material provides better performances in the current sensitivity.

The metal-semiconductor work-function accounting doesn’t affect the current at these high levels of concentrations ($2 \ldots 4 \times 10^{21} \text{ cm}^{-3}$), while the interface charge changes the drain current shape and range from $\sim 6 \text{ nA}$ to $\sim 5100 \text{ nA}$ at the same geometry and external stimulus, due to the initial electrons accumulation.

If in the NOI structure with 400 nm oxide thickness, $N_O = 2 \times 10^{21} \text{ cm}^{-3}$, ideal interfaces and no quantum option in the models statement the drain current varied between 7 nA to 1.8 nA for $V_C = 0 \ldots 5 \text{ V}$, in the NOI structure with 50 nm oxide thickness, $N_O = 4 \times 10^{21} \text{ cm}^{-3}$, real interfaces characterized by $Q_0 = 5 \times 10^{10} \text{ e/cm}^2$, $\Phi_{\text{MS}} = -0.55 \text{ V}$ and N.Dort option in the models statement, the drain current varied between 70 nA to 57 nA for $V_C = 0 \ldots 5 \text{ V}$. The gate leakage currents are far away from the breakdown conditions in both cases (2 fA ... 10 pA), where the sizes were the same for the NOI investigated nanotransistors: $x_{n} = 4 \text{ nm}$, $y_{n} = 10 \text{ nm}$, $z_{n} = 10 \text{ nm}$, $y_{p} = 0 \text{ nm}$, $d = 3 \text{ nm}$. In conclusion, the Van Dort quantum model has affected the current confinement through the NOI nano-device, considering an effective broadening of the band-gap near surface. This hypothesis was validated by the simulations results of the currents. All the previous corrections are valuable tools in the transistor design and manufacturing.

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