Live Demonstration: A Scaled-Down Version of the BrainScaleS Wafer-Scale Neuromorphic System

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I. DEMONSTRATION SETUP

This demonstration is based on the wafer-scale neuromorphic system presented in [1], [2] and [3]. One wafer of this system contains 384 analog network chips (ANC) for a total of 40 M synapses and 200 k neurons. 12 FPGA boards hosting 48 digital network chips (DNC) [4] connect the wafer to outside stimuli by 768 2 Gb/s serial links. Since it is not feasible to bring a wafer module to the conference, a scaled-down demonstrator system was prepared, containing one FPGA board, one DNC and eight ANC chips (Fig. 1). The FPGA connects to a host PC via Gbit Ethernet and an oscilloscope will be used to visualize the analog signals within the network chips. The total setup will contain nearly one million individually programmable synapses and 4k neurons. Each neuron can be separately configured by 24 analog parameters. The whole system can emulate biological neural networks up to $10^5$ times faster than biological real time.

II. VISITOR EXPERIENCE

With the setup described above the visitors will get an impression of the different levels of signal processing taking place in large scale accelerated neuromorphic hardware. It will be possible to visualize the electronic equivalent of neural action-potentials and membrane voltages and to compare them to numerical simulations, demonstrating that neuromorphic hardware can be used as an alternative for emulating biological neural networks (see Fig. 2).

Throughout the system different encodings are used, allowing each component to keep up with the high event rates present in an accelerated neuromorphic system:

- spike trains in digital memory within the FPGA, encoded as a list of neuron numbers and event time stamps
- packet-based transport of neural events, coded as neuron number and event time, in-between the FPGA and the DNC, as well as the DNC and the ANC
- continuous-time digital event communication within the ANC (or across the whole wafer in the wafer-scale system)
- continuous-time analog transmission of synaptic currents to the target neuron

The demonstration setup will allow the visitors to monitor and partially manipulate the neural events at every level. They will get an insight into the complex interplay between packet-based and real-time communication necessary to combine continuous-time mixed-signal neural networks with a packet-based transport network. Several network experiments implemented on the setup will be accessible for user interaction.

REFERENCES


The simulator used was BRIAN: http://www.briansimulator.org.

Fig. 1. The demonstrator system: eight ANCs, DNC and FPGA board.

Fig. 2. Comparison of membrane traces and output spike times of a Poisson-stimulated analog neuron and a numerical simulation.