Abstract—A synthesized compact model of substrate coupling resistance for lightly doped substrate processes is proposed. The model incorporates all geometrical parameters including geometrical mean distance with a few process-dependent fitting coefficients. The model accuracy is shown to be within 15% error using the measurement data from two test chips, one in a customized lightly doped process and the other one in a 0.18-µm BiCMOS lightly doped process. Substrate noise distribution on a 2 mm by 2 mm chip with 319 substrate contacts is shown with the calibrated SCM model.

I. INTRODUCTION

In mixed-signal ICs substrate noise coupling has been recognized as a major problem. The switching activity of digital circuit inevitably generates undesired noise current. It is injected into and propagates through the substrate to degrade the performance of sensitive analog or RF circuits residing on the same substrate wafer. There are three major noise injection mechanisms, i.e., impact ionization due to hot electron effects, capacitive coupling through reverse biased source/drain-bulk junction capacitance, and supply noise at power and ground contacts mainly due to inductive \( L \frac{di}{dt} \) noise. As technology scaling advances to current technology node, the impact ionization and source/drain junction capacitive coupling have already become negligible compared to supply noise at power and ground contacts [1]. This will remain so in the future technology nodes.

Many 3-D mesh-based numerical extraction methods using FDM, FEM, or BEM have been reported [2]-[4]. Macro model in compact form for heavily doped substrate has also been proposed in [5] and later improved in [6]. Lightly doped substrates are widely used in today’s mixed-signal technology. The high resistivity of substrate provides better noise isolation and suppresses more eddy current in substrate to make it possible to integrate high quality passive components. There have been analysis and experimental work reported, e.g., [7][8]. However, a more attracted substrate model should be truly scalable in layout geometry given process.

In this paper, a synthesized compact model (SCM) is introduced with the near and far field implication explained and the measure of distance redefined in section II. Test chips containing SCM test structures in two lightly doped processes are discussed in section III. Measurement data from both chips are compared with the SCM modeling results in section IV. A full-chip level noise floor planning analysis example is given to show the model application in section V.

II. SYNTHESIZED COMPACT MODELING TECHNIQUE

A. Substrate Coupling in Near Field and Far Field

Although it is widely believed and generally true that the substrate coupling between two substrate ports decreases when the separation increases, the subtleties of the difference in near field region and far field region behavior has been less well recognized. Approximately depending on the relative aspect ratio of the size of two ports and the separation between them, the coupling decaying trend behaves differently in two regions. This can be explained geometrically and physically. From the layout geometry point of view, when the separation is large enough compared to the contact size, both contacts see each other as lumped points. By contrast when two contacts are close to each other, the spreading effects of the current flow are more significant. Hence, the shape, size, alignment and relative position all contribute to the overall coupling strength. From device and electromagnetic physics point of view, in far field region the magnitude of \( \vec{E} \) field drops off at a rate proportional to \( 1/r \) whereas in near field region it drops off at a rate proportional to \( 1/r^2 \). Meanwhile, in the area close to the contact, the equal potential lines are spaced closely implying a high voltage drop and therefore a high current density there. So when the separation is relatively large, the far field effect dominates along most part of the coupling path and the near field effect dominates in the area close to the noise aggressor and victim; when the separation is small, the near field effect dominates. As a result, when the separation is small the coupling strength is stronger than usually believed and when the separation is large the coupling strength asymptotically approaches to a saturation level as opposed to the usual belief that it decays significantly with increasing distance.

B. Re-definition of Distance: Geometric Mean Distance

When two contacts are well aligned it is convenient to use edge to edge distance as the definition of distance, spacing, or separation. However, this definition may become ambiguous when two contacts are arbitrarily positioned. Fig. 1 illustrates
such an example.

![Fig. 1. Illustration of using geometric mean distance to define the separation.](image)

Hence, a more appropriate and unified definition of distance needs to be introduced so that this geometrical parameter can be used to develop and be included in the scalable compact model. For this purpose, the concept of geometric mean distance (GMD) is used here. Fig. 1 shows a configuration of two rectangle contacts. The GMD distance, \( d_{\text{GMD}} \), is defined as following:

\[
d_{\text{GMD}} = \frac{1}{4} \left( \int_{x_1}^{x_2} \int_{y_1}^{y_2} \left( x_2 - x_1 \right) \, dx \cdot dy \right)^{\frac{1}{2}}
\]

where \( r \) is the distance between point \((x_1, y_1)\) and \((x_2, y_2)\), \( W_1 \) and \( W_2 \) are the widths of two contacts, \( L_1 \) and \( L_2 \) are the lengths of two contacts. GMD has been used in inductance computation for a long time [9]. By definition, it takes into account the area, perimeter, and relative position of two contacts particularly pronounced in the near region. This is also a favorable property for the development of compact models for substrate resistance. The formula in (1) can be further simplified by various approximating compact closed-form expressions [9].

C. Compact Substrate Resistance Model

The proposed compact model of substrate coupling resistance between two arbitrarily sized contacts reads

\[
R_{ij} = \beta \left[ \ln(d_{ij} + 1) \right]^{\alpha_i} \cdot (s_i + s_j)^{\alpha_2} \cdot (p_i + p_j)^{\alpha_3}
\]

where \( d_{ij} \) is the geometric mean distance between two contacts, \( s_i \) and \( s_j \) are the areas of contact \( i \) and contact \( j \), \( p_i \) and \( p_j \) are the perimeters of contact \( i \) and contact \( j \), \( \beta, \alpha_i, \alpha_2 \) and \( \alpha_3 \) are four fitting coefficients, characterizing the substrate coupling resistance’s dependence on substrate doping profiles, separation between two contacts, contact areas, and contact perimeters, respectively. These fitting parameters are independent of layout geometry but are only process-dependent. They can be obtained by rigorous 3-D EM or device simulation results and further calibrated by measurement data from SCM test structures on test chips.

III. SCM TEST CHIPS

To verify the SCM model step by step, two different lightly doped processes have been used to fabricate the test chips.

A. Test Chip I: Customized Lightly Doped Process

This customized process was developed at the Stanford Nano-Fabrication (SNF) facility. The bulk silicon is uniformly doped at \( N_s = 1 \times 10^{15} \text{ cm}^{-3} \). The N well thickness is 1 µm with peak concentration of \( N_{d,\text{peak}} = 1 \times 10^{15} \text{ cm}^{-3} \). The starting substrate resistivity is 11-16 \( \Omega \cdot \text{cm} \). The sheet resistances of thin film P-well and N-well are 315±110 \( \Omega / \square \) and 360±110 \( \Omega / \square \), respectively. Fig. 3 shows the die photo of the chip, which consists of reduced set of SCM test structures and other mixed-signal circuit blocks. This paper focuses on the SCM test structures only and other portions of the chip will be reported in a later phase.

IV. EXPERIMENTAL VERIFICATION OF SCM MODEL

A. Measurement Results for SCM Structures in Test Chip I

Fig. 4 shows the comparison between the measurement data and the SCM modeling results for sample structures in array 1-3. Fig. 4(a) shows the substrate resistance between two identical square contacts as a function of separation for contact width \( W = 18, 24, 30, 36, \) and 42 µm. Fig. 4(b) shows the substrate resistance between a square contact of 6 µm \( \times \) 6 µm and a rectangle contact of 6 µm \( \times L_2 \), where \( L_2 = 18, 24, \) and 42 µm. It can be seen that in both cases the coupling resistance varies with increasing separation in a similar manner, i.e., increasing much faster than linearly for relatively smaller separations and continuing to increase but at a slower, almost linear rate for relatively larger separation. The SCM model agrees with the measurement data nicely. Typical error falls within 5% with a few exceptions of about 10%. It is
interesting to note that the SCM model consistently works well in both near field region and far field region.

Fig. 4. Measurement data and modeling results of sample test structures in test chip I. (a) Two identical square contacts. (b) Square contact to rectangle contact.

The configuration of two contacts unaligned is depicted as the inset of Fig. 5. The right contact is 6 µm × 90 µm whereas the left contact is W_l × 6 µm with the offset varying from 0 to 84 µm. The upper and lower set of curves are for W_l=24 µm and 60 µm, respectively. Note that the strongest coupling occurs when the left contact is center aligned to the right one. For this particularly configuration the coupling varies by 10% when the left one moves towards either end alignment with the right one. Fig. 6 illustrates the configuration of two contacts unaligned with even more offset, namely, super offset. In this case, the ambiguity of using regular edge to edge distance can be clearly seen.

Fig. 5. Contacts unaligned with offsets in test chip I.

A typical configuration of guard ring is depicted in Fig. 7. The substrate noise isolation can be measured by the ratio of noise sensed by the victim and the source noise level at the aggressor. Fig. 7 shows that the noise isolation in dB is roughly proportional to the guard ring width. In this particular case, every 2 µm increase of guard ring width gains about 2 dB more noise isolation. Different placement of noise victim inside guard ring can also affect the noise isolation, as shown in Fig. 8. The isolation worsens as the victim moves from position 1 to 4. However, as the victim moves from position 4 to 7 the isolation actually enhances rather than worsens. Closer spacing to the guard ring means the victim locates in the vicinity of guard ring biasing area. An improvement of 2 dB is observed when the victim moves from position 4 to 7.

Fig. 6. Contacts unaligned with super offset in test chip I.

B. Measurement Results for SCM Structures in Test Chip II

In this 0.18-µm BiCMOS process the minimum unit P+ contact size is 0.4 µm by 0.4 µm. Fig. 9 summarizes the comparison of measurement data and SCM modeling results for relatively small contact structures. Fig. 9(a)-(d) show the substrate resistance for P+ contacts sized at 1 by 1 unit, 4 by 4 unit, 3 by 10 unit, and 4 by 20 unit, respectively. The SCM model has good agreement with the measurements with mean error of 7% and maximum error 11%. Fig. 10 shows the results for the relatively large contact structures. For these structures, the substrate resistance is in the order of 10^3 Ω. The average error is 10% with maximum error 15%.

Fig. 7. Noise isolation sensitivity on guard ring width.

Fig. 8. Noise isolation sensitivity on victim’s location inside guard ring.

Fig. 9. Measurement data and SCM model for test chip II. Each contact is sized at W × L. (a)W = 0.4 µm, L = 0.4 µm. (b)W = 1.6 µm, L = 1.6 µm. (c)W = 1.2 µm, L = 4.0 µm. (d)W = 1.2 µm, L = 8.0 µm.
V. APPLICATION EXAMPLE

The SCM model calibrated by measurements from test chip II is used to perform a full chip level noise analysis here. Fig. 11(a) shows the layout of the test chip II discussed above. Fig. 11(b) shows totally 319 p+ substrate contacts and two major digital noise sources recognized using an SCM-enabled CAD tool [10].

It took 97 seconds on a SunBlade 100 workstation to get a resistive substrate network using the SCM model. Assuming all the substrate contacts and the backside are grounded, if the perturbation of 300 mV is injected at aggressor A and 200 mV is injected at aggressor B, the surface noise distribution can be computed using the generated network. Fig. 12 and 13 show the resulted noise distribution and equal noise level contour. It can be seen that the noise is high in the vicinity of noise source locations and decays rapidly approaching a global saturated noise level at about 30-35 mV. Similar observation has been suggested from very simple configuration in [11].

VI. CONCLUSION

In this paper, the synthesized compact model (SCM) for substrate resistance in lightly doped processes has been proposed. Measurements from test chips in two lightly doped substrate processes are presented, validating the model’s accuracy to be within 15%. The substrate noise analysis results in a full-chip example are obtained. The SCM model should be useful in mixed-signal substrate noise analysis. Future work includes measurements of other portions of test chip II using the calibrated model.

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REFERENCES