Performance Evaluation of an Automatic Impedance Synthesizer based on RF Switches

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Abstract—This paper presents a new design of an automatic impedance synthesizer based on RF switches and its performance. A study about the implementation has been carried out and two prototypes of 50 Ω and 75 Ω of characteristic impedance have been successfully constructed. As switching elements in the tuning network we employ GaAs MMIC RF switches. An evaluation of impedance matching zones in the Smith chart has been carried out using simulations, taking into account both the return losses and the dissipative losses due to the physical implementation of the prototypes. Finally two prototypes of 50 Ω and 75 Ω have been constructed, verifying its correct operation.

Index Terms—Antenna tuning unit, ATU, impedance synthesizer, tuning networks, RF switches.

I. INTRODUCTION

Impedance tuning networks are widely used in electronic applications, such as antenna tuning units (ATUs), RF power amplifier designs or power transistor characterization. Unlike impedance transformers, impedance tuning networks or impedance synthesizers can generate a set of possible impedances changing the state of some of the elements of the network.

The input impedance of the antenna is one of the most changing parameters as a consequence of the environment variability in communication mobile systems. This fact leads to two main factors. First, the power module will not perform at optimal efficiency under load variations, and, second, the radiated power decreases due to the reflected power, with an increase in the energy consumption or a deterioration in the quality transmission and even in the power transistor.

An automatic impedance synthesizer can help to address this problem. The II-network topology has been widely used in literature [1]–[6] as the basic structure of tuning networks. This solution is simple and allows to synthesize whatever complex impedance. As the frequency increases, this topology based on lumped elements is not efficient and it is necessary to apply different techniques. Tuning networks based on transmission lines or MMICs for GHz-bands can be found in recent literature [7]–[11]. There are also differences between the mechanism used to generate the sets of complex impedances. The use of varactors in tuning networks [1], [7], [12]–[16] allows a theoretical infinite tuning range, but has the disadvantage of the analog control circuitry necessary to control the device and the low RF power range. To solve this issue, digital control based on RF switches or MEMS switches is also highly extended [3], [4], [6], [9], allowing an easy integration with nowadays digital radio devices.

In this paper, an automatic impedance synthesizer based on GaAs MMIC RF switches, using lumped elements is presented. It is designed to operate around the 450 MHz frequency band and can easily be digitally controlled.

The paper is organized as follows. In Section II the topology and principles of the synthesizer are presented as well as the design and optimization process and some preliminary results. A study of the impedance matching coverage has been carried out in Section III. Section IV presents the constructed prototypes and its verification. The conclusions are summarized in Section V.

II. TOPOLOGY

The design of the impedance synthesizer starts from the low pass II-network topology, widely used in tunable impedance transformers [1]–[6]. It consists essentially on a shunted capacitor, a series inductor and another shunted capacitor. This network allows ideally to transform whatever presented complex impedance into another desired one, selecting properly the network components.

This initial topology is modified replacing each of the capacitors with a bank of four shunted capacitors of different values, and the inductor with another capacitor bank and two impedance inverters to emulate the inductive behavior of the network [2], [6]. Due to the frequency at which the prototype operates is around 450 MHz, lumped elements are used. Fig. 1 shows a schematic picture of the proposed topology.

The structure of the capacitors bank is detailed in Fig. 2. Each one of the four capacitors in the bank can be activated or deactivated via RF switches. If the RF switch is on, the
capacitor adds its capacitance value to the network, whereas if the RF switch is off, ideally the capacitor and the RF switch do not influence the rest of the network.

We employ in this design GaAs MMIC RF switches of Hittite because of its good properties in terms of:

- Good isolation (30 dB).
- Low insertion losses (0.4 dB) and return losses (30 dB).
- High linearity at high power levels ($P_{1dB} = 30$ dBm, $IP3 = 45$ dBm).
- Low power consumption ($10 \mu A$) and broadband behavior (up to 3 GHz).
- Fast switching times (3-10 ns).

The switches can be digitally controlled, making easy the integration with a digital processor or FPGA. The final implementation of the tuning network uses 12 capacitors, grouped into three banks, allowing synthesize up to 4096 different complex impedances. The idea is to cover the maximum area in the Smith chart, that is, to be able to synthesize as many different complex impedances as possible. As the number of possible impedance is high, it will be necessary some kind of algorithm to choose properly the desired impedance, according to some criteria, typically minimizing the reflected power from the antenna in ATU applications [6]. Another requirements, e.g. linearity or adjacent channel interference can also be taken into account. The inclusion of digital processors in today-radio devices makes feasible the implementation of these algorithms, although they are not matter of this paper.

### A. Design process and simulation results

The initial proposal for the capacitor values of the network was a exponential progression in each bank, so the value of a capacitor located in each of the banks was given by

$$C_n = k \cdot 2^n \text{ (pF)}$$

with $n = 1, 2, 3, 4$, and $k = 1$ initially. With these values, the dynamic range is set by the maximum capacitance in each block,

$$C_{\text{max}} = \sum_{n=1}^{4} C_n \text{ (pF)}$$

and the resolution by the relation between the maximum capacitance and the number capacitors [3]

$$\Delta C = \frac{C_{\text{max}}}{2^{n-1} - 1}$$

Under ideal conditions (ideal capacitors, inductors and RF switches), and with these proposed values of $C_n$ with $k = 1$, the set of synthesizable impedances by the tuning network covers almost completely the Smith chart as it can be seen in Fig. 3.

However these values do not lead to optimal distribution and coverage of impedances in the Smith chart when all the parasitic effects, both of the lumped elements and those related to the PCB design, are considered in simulation. In fact, a considerable reduction of the coverage area takes place. This reduction can be observed in Fig. 4. In this situation, the 4096 complex impedances have collapsed in a small region of the Smith chart, leading to a non-satisfactory result in terms of area coverage.

Additionally we propose the construction of two prototypes with different characteristic impedances $Z_0$, of 50 and 75
TABLE I: Capacitor values for both prototypes.

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Bank 1</th>
<th>Bank 2</th>
<th>Bank 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 (pF)</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>C2 (pF)</td>
<td>2</td>
<td>2</td>
<td>3.9</td>
</tr>
<tr>
<td>C3 (pF)</td>
<td>3.9</td>
<td>2</td>
<td>8.2</td>
</tr>
<tr>
<td>C4 (pF)</td>
<td>8.2</td>
<td>3.9</td>
<td>18</td>
</tr>
</tbody>
</table>

Ω, both widely used in communication systems. Simulations of the complete set of possible synthesized impedances for both the 50 and 75 Ω circuits at the design frequency of 450 MHz are shown in Fig. 5. Simulations have been carried out with AWR Microwave Office, using real models for all the components as well as for the PCB design. A large set of impedances can be synthesized for both situations, however the coverage in the Smith chart is higher in the 75 Ω prototype. This fact is due to the use of narrow lines in the main branch of the network, which leads to a higher characteristic impedance, and a higher inductive component. This last factor makes the set of synthesizable points to move towards the extremes of the Smith chart, achieving a higher density of possible synthesizable impedances.

III. MATCHING REGIONS

A. Coverage based on return losses

The complex conjugate of the synthesizable impedances set showed in Fig. 5, corresponds to those values of impedance, (antenna input impedance in ATU applications) which can be perfectly matched in the sense of classic power matching. It can be also very useful to see what happens with other impedances which are not represented in Fig. 5. Although we cannot find a perfect matched impedance for them, it is very likely to find an impedance which provide an acceptable matching value in terms of return losses. With this idea, a generalized reflection coefficient $\Gamma_g$ is defined as follows

$$\Gamma_g = \frac{Z_{\text{synthesized}} - Z_{\text{load}}^*}{Z_{\text{synthesized}} + Z_{\text{load}}}$$  \hspace{1cm} (4)

where $S_{11}$ and $S_{21}$ are the correspondent S-parameters of the tuning network scattering matrix. When real models for the components and for the PCB design are used, Eq. 6 is not correct, since it is valid only for lossless networks, so the dissipative losses associated to the network in dB can be formulated as

$$DL(\text{dB}) = 10 \log(1 - |S_{11}|^2 - |S_{21}|^2)$$  \hspace{1cm} (7)

The origin of this losses can be grouped in two categories. The former, take into account the losses of the electrical components, namely capacitors, inductors and RF switches, and will be influenced mainly by the non-zero resistance of the RF switches in the on state, and the equivalent series resistance (ESR) of the capacitors. The latter are associated to the printed circuit board design and depends on the construction process and materials for the PCB. In this design, low cost FR4 substrate (typical $\varepsilon_r = 4.5$, $\tan\delta = 0.04$) has been used. Besides, dissipative losses of the network will not be constant but will depend on the state of the RF switches. Those situations which need more RF switches activated to obtain

This value, and its representation as return losses as

$$RL(\text{dB}) = 20 \log |\Gamma_g|$$  \hspace{1cm} (5)

measure the difference between the synthesized impedance ($Z_{\text{synthesized}}$) by the device and the load impedance ($Z_{\text{load}}$) which is presented to the device at one of their ports. In Fig. 6 the impedance matching area with return losses less than $-10$ dB is presented. These outcomes are sound with those presented in Fig. 5, since the matching area for the 75 Ω prototype is larger than the 50 Ω prototype’s area. In the case of the 75 Ω circuit the coverage region includes almost all impedances inside a circle defined by a VSWR of 7:1. In the case of the 50 Ω circuit the coverage is not so regular but includes also a large region of matchable impedances.

B. Losses Analysis

Under ideal conditions, which means no network losses (Fig. 3), this reciprocal tuning network meets the equation

$$|S_{11}|^2 + |S_{21}|^2 = 1$$  \hspace{1cm} (6)

where $S_{11}$ and $S_{21}$ are the correspondent S-parameters of the tuning network scattering matrix. When real models for the components and for the PCB design are used, Eq. 6 is not correct, since it is valid only for lossless networks, so the dissipative losses associated to the network in dB can be formulated as

$$DL(\text{dB}) = 10 \log(1 - |S_{11}|^2 - |S_{21}|^2)$$  \hspace{1cm} (7)

Fig. 5: Set of synthesizable impedances represented on the Smith Chart, at a frequency of 450 MHz.

Fig. 6: Impedance matching area corresponding to a return losses less than $-10$ dB for both prototypes.

(a): 50 Ω.  \hspace{1cm} (b): 75 Ω.
Fig. 7: Impedance matching area corresponding to a return losses less than $-10$ dB and losses less than 2 dB for both prototypes.

the desired matching, will have associated larger dissipative losses since the resistance of the RF switch will be added up to the ESR of the capacitor. It can be seen however, the more active RF switches on a single capacitor bank, the less the equivalent resistance will be, calculated as the parallel of four resistances. The impedance inverters used to emulate the inductive behavior will also add some losses.

To quantify the effect of the losses in the tuning network, we simulate with AWR Microwave Office the circuit using real models for the components and for the PCB layout design. We add to the graphics showed in Fig. 6 another constrain relative to the previously presented dissipative losses, represented by Eq. 7. Then, Fig. 7 shows the impedance matching area corresponding to return losses less than $-10$ dB and dissipative losses less than 2 dB for both the 50 and 75 Ω prototypes. In both situations, the matching represented area decreases in comparison with Fig. 6, where only the return losses criteria were considered. Additionally, although in Fig. 6 a large coverage area can be observed for the 75 Ω circuit, in Fig. 7 this region is smaller than in the 50 Ω prototype. This fact is due to the higher losses associated to the narrower microstrip line used in the 75 Ω prototype, and whose attenuation due to conductor losses $\alpha_c$, is given approximately by [17]

$$\alpha_c = \frac{R_s}{Z_0 W}$$

where $R_s = \sqrt{\frac{\omega \mu_0}{2\sigma}}$ is the surface resistivity of the conductor and $W$ is the width of the microstrip line.

IV. PROTOTYPES CONSTRUCTED AND VERIFICATION

Fig. 8 shows a picture of the 50 Ω prototype constructed. Its size is approximately 6 × 7.5 cm. The correct operation of both prototypes is verified, comparing the simulation results with the real measurements using a network analyzer. A sample of these measurements is shown in Fig. 9. Simulation and measurement outcomes for the $S_{11}$ and $S_{21}$ parameters for different states of the RF switches.

V. CONCLUSIONS

We have presented in this paper the design and evaluation of two impedance synthesizers based on RF switches. Simulation results of impedance matching areas based on return losses
and dissipative losses have been discussed. Under the return losses criteria, a large coverage area is obtained for both prototypes, specially for the 75 Ω one. Adding the network losses constrain, a reduction on the coverage area can be appreciated, although acceptable results keep up. Finally, two prototypes have been constructed and its correct operation verified correctly, comparing simulation and measurements of the prototype based on S-parameters.

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