Time-To-Latch-Up Investigation of SCR Devices as ESD Protection Structures on 65 nm Technology Platform

A. Tazzoli¹*, M. Cordoni², P. Colombo², C. Bergonzoni², G. Meneghesso¹

¹University of Padova, Department of Information Engineering, Via Gradenigo 6/b, 35100, Padova, Italy
²STMicroelectronics, Agrate Brianza (Mi), Italy
*e.mail: augusto.tazzoli@dei.unipd.it; tel: +39 049 8277664; fax: +39 049 8277699

Abstract

The purpose of this work was to study the influence of different layout parameters on the electrical performances and Time-To-Latch-Up (TTLU) by means of the injection of substrate current on SCR devices to be used as ESD protection structures for the 65 nm Flash memory technology platform. Low (1.2 V) and high (5.0 V) voltage class devices were studied in DC and 100 ns TLP regime, and an ad-hoc setup was developed to investigate TTLU as a function of the injected current needed to latch-up HV-SCRs.

1. Introduction

Latch-up is a state where a semiconductor device undergoes a high-current state as a result of interaction between a PNP and an NPN bipolar transistors, that can be both natural to the technology (SCR), or parasitic devices (CMOS). Once latch-up has begun, the only way to stop it is to reduce the current below a critical level, usually by removing power from the circuit. The result of latch-up is at the minimum a circuit malfunction, and in the worst case, the destruction of the device [1]-[3].

In this work we studied the influence of different layout parameters on the electrical performances and Time-To-Latch-Up (TTLU) by means of the injection of substrate current on SCR devices to be used as ESD protection structures for the 65 nm Flash memory technology platform. Low (1.2 V) and high (5.0 V) voltage class devices were studied in DC and 100 ns TLP regime, and an ad-hoc setup was developed to investigate TTLU as a function of the injected current needed to latch-up studied HV-SCRs.

2. Device Description

In this work we have analyzed the ESD robustness and the Time-To-Latch-Up (TTLU) of SCRs for both low voltage (LV, 1.2 V) and high voltage (HV, 5.0 V) classes. Figure 1 shows the simplified cross section of tested devices, superimposed with the corresponding electrical circuit.

Fig. 1. Schematic section and electric circuit of studied SCRs.

Two implants were added in studied SCRs, in order to inject current by the substrate and better investigate their sensitivity to latch-up phenomena. Such implants were contacted by means of the pads R and D. The p+ contact (pad R) is similar to the substrate-triggering diffusion proposed in [4]-[6]. Tested SCRs are different from each other for the following geometrical parameters: L (from 0.17 to 2.64 μm), the distance between the PNP collector and the NPN emitter, A (from 2.56 to 6.00 μm), the distance between the cathode p+ contact and the n-well, and B (from 2.56 to 9.00 μm), the distance between the anode n+ contact and the n-well. The distance A affects the resistance R2, whereas the distance B affects the resistance R1. The distance L influences the behavior of the two BJTs, in particular the transistors gain, since it determines the base widths of the NPN and of the PNP. Another difference is the presence of the N-Buried layer (NB), providing a deep N implant, used to built isolated...
substrate portion from the bottom. Conventional N-Well of a CMOS process is then used to isolate this substrate along all other sides. HV-SCR structures provide isolated substrate for the lateral NPN of the SCR (embedding n+ and p+ cathode diffusions). In total 28 different geometries per class were studied.

2. DC and TLP Characterization

A preliminary characterization of SCRs in DC regime was performed with an HP 4145B Semiconductor Parameter Analyzer. Devices were measured in DC regime forcing current to the anode pad (A) vs. the cathode one (K) in order to allow tested SCRs to snap-back from the high-impedance to a low-impedance one (from the triggering to the holding voltage). The high-current behaviour of tested SCRs was tested by means of a 100 ns TDR-TLP. SCRs life state was analyzed by means of leakage current measurement @ 1.2 V for LV devices, and @ 5 V for HV ones) after each TLP pulse. An example of the I-V curves extracted in TLP regime is shown in Figure 2.

![Fig. 2. Example of I-V and leakage curve shown by SCR-LV.](image)

The main results from DC and TLP regime characterizations are: (i) as L increases, the holding voltage and the failure current increase, and the device resistance decreases. (ii) As A increases, so do V_Hold and slightly I_Fail. Whereas, if B increases, V_Hold and the device resistance (on-state) decrease, and I_Fail increases. (iii) L, A and B do not really affect the triggering voltage, that instead is strongly modified by the presence of the N-buried layer. (iv) The N-buried presence makes the trigger voltage be lower if compared to the standard devices. This difference is about 2.5 V for LV-SCRs, and about 9 V for HV devices. (v) All devices have shown an abrupt failure.

3. Time-To-Latch-Up Characterization

We have investigated the latch-up sensitivity of tested SCRs studying the TTLU as a function of the injected current into the R pad. When a current is injected in the p+ diffusion (pad R), it flows to the cathode getting through the device. This current is responsible for the voltage drop on the resistance R2 (see Fig. 1), voltage that causes the NPN to turn on, when it is above a certain value depending from the device. In the case that also the PNP turns on, and VSCR (the voltage applied to the SCR) is above the holding voltage V_Hold, latch-up is likely to occur, and the device remains turned-on as long as the supply is applied to the SCR, or until the device failure. The setup used for such measurements was made of a HP 8110A Double Pulser, a Tektronix TDS654C 4-Channels Oscilloscope, and the LabView Virtual Instrument realized on purpose to acquire the data. The Virtual Instrument was made to control the HP 8110A, used to generate a voltage pulse, 1.2 μs long, to supply the nominal voltage to the SCR under test (5 V for HV devices), and a variable amplitude second pulse 900 ns long, delayed of 100 ns from the first one, applied to the R pad. The choice of these pulses times was made to do not damage the devices, and also because, during preliminary tests, it was not noticed any latch-up event at longer times (at least considering the maximum current levels obtainable with the HP 8110A, about 250 mA). An example of voltage and current waveforms (VSCR, ISC, VR, IR) acquired during TTLU tests is shown in Figure 3.

![Fig. 3. Example of latch-up waveforms: 1) start of the first pulse; 2) begin of the second pulse; 3) latch-up occurrence; 4) end of the second pulse (on pad R); 5) end of the first pulse (SCR bias). Note that after 4 the SCR is ON and VSCR is equal to V_Hold.](image)
Applying increasing voltage pulses on the R pad (that means increasing the injected current on the substrate) and extracting the corresponding data, TTLU versus injected current ($I_{\text{latch-up}}$) curves were obtained.

Three measurements were repeated for each value of the substrate injected current, and a typical behavior shown by tested SCRs is reported in Figure 4.

From the graph it can be noticed that the TTLU decreases as the current increases, and it saturates to a defined time value (about 40 ns). Furthermore, injected currents lower than 50 mA are not enough to leave the SCR turned on (latch-up condition). The different TTLU curves shown by a selection of tested SCR-HV devices are reported in Figure 5. From TTLU measurements, the following considerations can be made:

(i) SCRs with minimum length $L$ and N-Buried layer were the most robust among all the tested ones, because they did not manifest any latch-up issue with the used setup (up to 250 mA).

(ii) HV-SCRs with maximum $L$ length were the most robust among the devices that showed latch-up, in particular the P-type, where the N-well is closer to the cathode.

(iii) Four typologies, above a repeatable injected current value, immediately manifest latch-up when the pulse on R starts.

(iv) Devices without the N-Buried layer are generally more susceptible to latch-up events since their corresponding $I_{\text{latch-up}}$ value is lower.

(v) Smaller the value of $A$, the distance between the cathode p+ contact and the n-well, the higher $I_{\text{latch-up}}$ needed to leave the device turned-on (latched). The LV devices were taken off from this analysis, because their holding voltage was higher than the supply voltage (1.2 V). In this condition they cannot stay active when $I_p$ pulse ceases, and so they did not show any latch-up condition.

4. Conclusions

In this work we have investigated the influence of different layout geometrical parameters on the electrical characteristics of SCRs based ESD protection structures. Furthermore, the Time-To-Latch-Up was investigated for the different geometries injecting an increasing current to the SCR substrate up to the occurrence of the latch-up condition. Obtained results can make possible to establish proper guidelines for better Latch-Up immunity of ESD SCR-based protections. Furthermore, not less important, the experiment discussed has shown a very promising method in analyzing Latch-Up induced effects.

References