A Low-Voltage CMOS Multiplier and Its Application to a 900MHz RF Downconversion Mixer

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ABSTRACT

A low-voltage, low-power analog multiplier operating at 1.2 V is presented. The multiplier is composed of a pair of voltage-to-current converters and a pair of voltage followers. The current produced is then added in resistors to produce the voltage output. The circuit multiplies the incoming 900 MHz RF signal with an 800 MHz local oscillator signal to produce a 100 MHz IF output. The circuit was designed using standard 0.35 µm CMOS technology. Simulation results indicate an input referred IP3 of 1 dBm and a spur free dynamic range of 44 dB.

1. INTRODUCTION

The mixer is an indispensible block in receiver systems where its main function is to translate the incoming RF signal to an intermediate frequency signal for further processing. In the last years a lot of effort has been spent in the development of low-voltage CMOS RF mixers [1] – [5]. This has been driven by the demand for portable wireless communications systems. The design of portable sets follows the trends that include lower cost, longer battery life, smaller size and lower weight. In order to achieve this goal low-voltage low-power analog blocks are required.

In this paper we propose a low-voltage circuit capable of performing the analog multiplication of two differential input signals, with low-signal distortion and low-power dissipation. The most noticeable feature of the proposed structure is its low-voltage operation. It can operate at a supply voltage of 1.2 V while sustaining high linearity making it suitable for battery operated portable systems. The circuit has been designed for a 1.2 V, 900 MHz application in a standard 0.35µm CMOS process. The circuit is described in section 2. The simulation results follow in section 3, while a conclusion is given in section 4.

2. CIRCUIT DESCRIPTION

The circuit diagram of the voltage-to-current converter is shown in Fig. 1.

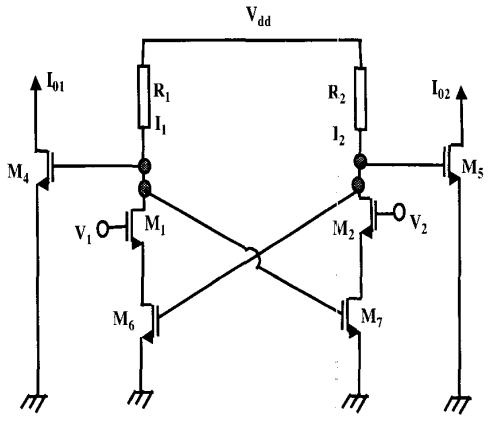

Fig. 1 – Schematic Diagram of the V-I Converter

The differential input swing of the circuit is limited by the threshold voltage of the core transistors M_1 and M_2, the voltage drop accross

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the resistors R_1 and R_2, and the drain-source voltage of the current sources M_6 and M_7. This results in a narrow differential input window for low-voltage applications. In order to increase the input swing transistors M_6 and M_7 are biased in the triode region and R_1 and R_2 are chosen such that the drain-to-source voltage of M_1 and M_2 are close to supply. The input transistors M_1 and M_2 are biased to operate in the saturation region. M_4 and M_5 produce currents I_{01} and I_{02} depending on their repective gate voltages. Thus the currents I_{01} and I_{02} are proportional to the input voltages V_1 and V_2 respectively.

Fig. 2 shows the complete mixer circuit. Two voltage-to-current converters are parallelly connected with a pair of voltage followers [6], M_3 and M_{10}. The source of the follower M_3 (M_{10}) and the sources of the transistors M_1 and M_2 (M_8 and M_9) are connected together.

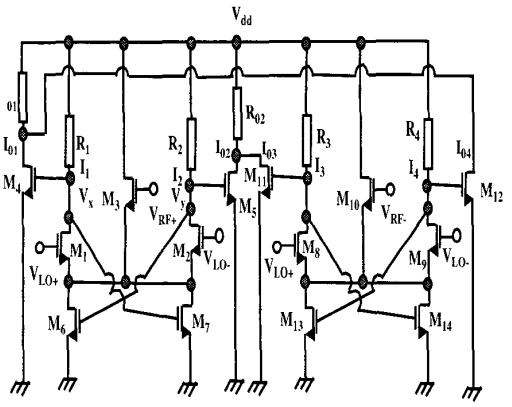

Fig. 2 – Schematic Diagram of Proposed Mixer

The current equation for the MOS transistor in saturation is approximately given by:

$$I_D = \frac{KW}{2L}(V_{GS} - V_{th})^2 \qquad (1)$$

where $K = \mu C_{ox}$, W and L are the width and length of the transistor respectively, V_{GS} is the gate to source voltage, and V_{th} is the threshold voltage. Assuming that the threshold voltages of all the NMOS are the same and K_{n1} is the transconductance parameter,$K_{n1} = K_{M1}W/L$ of M_1, M_2, M_3, M_8, M_9, M_{10}, then:

$$I_1 = \frac{K_{n1}}{2}(v_{LO+} - v_{RF+})^2 + \sqrt{2I_{M3}K_{n1}}(v_{LO+} - v_{RF+}) + I_{M3} \qquad (2)$$

$$I_2 = \frac{K_{n1}}{2}(v_{LO-} - v_{RF+})^2 + \sqrt{2I_{M3}K_{n1}}(v_{LO-} - v_{RF+}) + I_{M3} \qquad (3)$$

$$I_3 = \frac{K_{n1}}{2}(v_{LO+} - v_{RF-})^2 + \sqrt{2I_{M10}K_{n1}}(v_{LO+} - v_{RF-}) + I_{M10} \qquad (4)$$

$$I_4 = \frac{K_{n1}}{2}(v_{LO-} - v_{RF-})^2 + \sqrt{2I_{M10}K_{n1}}(v_{LO-} - v_{RF-}) + I_{M10} \qquad (5)$$

The voltages V_x and V_y can be found from the following equations.Assuming $R_1 = R_2$, which can be achieved with careful layout, then:

$$I_1 - I_2 = \left(\frac{V_{dd} - V_x}{R_1}\right) - \left(\frac{V_{dd} - V_y}{R_1}\right) \qquad (6)$$

$$I_1 - I_2 = \frac{V_y - V_x}{R_1} \qquad (7)$$

But $V_x = -V_y$, giving:

$$V_x = \frac{R_1(I_2 - I_1)}{2} \qquad (8)$$

and,

$$V_y = \frac{R_1(I_1 - I_2)}{2} \qquad (9)$$

The drain current through transistor M_4, I_{01} is given by:

$$I_{01} = \frac{K_{n4}}{2}\left(\frac{R_1(I_2 - I_1)}{2} - v_{th}\right) \qquad (10)$$

where K_{n4} is the transconductace parameter of M_4, $K_{n4} = K_{M4}W/L$.

Similarly, assuming that the K_{n4} is also equal to the transconductance parameter of transistors M_5, M_{11}, and M_{12}, and that $R_1 = R_2 = R_3 = R_4$,

$$I_{02} = \frac{K_{n4}}{2}\left(\frac{R_1(I_1 - I_2)}{2} - v_{th}\right) \quad (11)$$

$$I_{03} = \frac{K_{n4}}{2}\left(\frac{R_1(I_4 - I_3)}{2} - v_{th}\right) \quad (12)$$

$$I_{04} = \frac{K_{n4}}{2}\left(\frac{R_1(I_3 - I_4)}{2} - v_{th}\right) \quad (13)$$

The currents I_{01}, I_{04} and I_{02}, I_{03} are added in resistors R_{01} and R_{02} respectively giving an output voltage equal to:

$$v_{out} = R_{01}[(I_{01} + I_{04}) - (I_{02} + I_{03})] \quad (14)$$

where $R_{01} = R_{02}$. Assuming a perfect match this yields:

$$v_{out} = A(v_{LO+} - v_{LO-})(v_{RF+} - v_{RF-}) \quad (15)$$

where $A = -R_{01}R_1K_{n1}K_{n4}v_{th}$. Thus the output voltage is given by the multiplication of the two differential inputs together with the constant A.

In practical circuit implementations, linearity error could result from mobility reduction, channel-length modulation and the body effect. The first two effects depend on the quality if the process, while the body effect can be reduced by connecting sources and bulks of transistors. The technology that was used in this design does not allow different p-wells for NMOS devices. However, when the source voltages of the input transistors are close to the ground node the body effect can be reduced without this source-bulk connection.

3. SIMULATION RESULTS

The circuit has been simulated using a standard 0.35 μm double-poly, double-metal CMOS process. The input and output ports were matched to a 50 Ω termination. All simulations were performed using a 1.2 V supply voltage. The differential input sinewaves applied at the input terminals have an amplitude of ±200 mV and frequencies of 800 MHz and 900 MHz at terminals v_{LO} and v_{RF} respectively, producing an output at 100 MHz.

The circuit consumes approximately 12mW from the 1.2 V supply. Most of the power is consumed in the output stage as R_{01} and R_{02} must be small in order to get a good output match.

The linearity of the proposed multiplier was simulated by applying 900 MHz sinusoidal wave inputs having different amplitudes at the RF input port while keeping the local oscillator port at a constant sinusoidal voltage of 200 mV. For each amplitude of the RF input the maximum output of the required RF signal was plotted. Fig. 3 shows the simulated linearity characteristics of the mixer for an RF input varying between 0V and 300 mV.

In Fig.4 the output voltage signal for a 200 mV, 900 MHz RF input and a 200 mV, 800 MHz local oscillator input is given. Fig. 5 illustrates the output spectrum. It shows that the third harmonic component, at 300 MHz lies 44dB below the fundamental frequency signal, at 100 MHz. In Fig. 6 the output power is plotted against the input power indicating that the input referred third order intercept point is at 1 dBm.

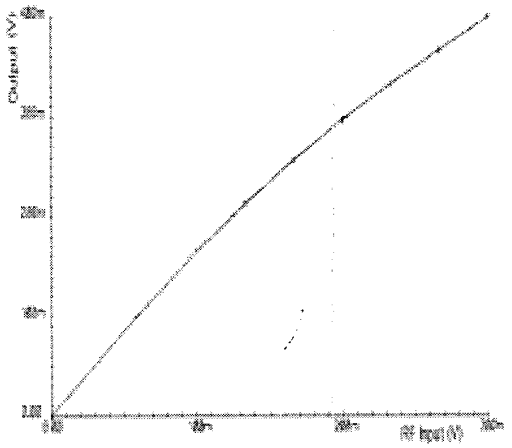

Fig. 3 – Linearity of the circuit at 900MHz

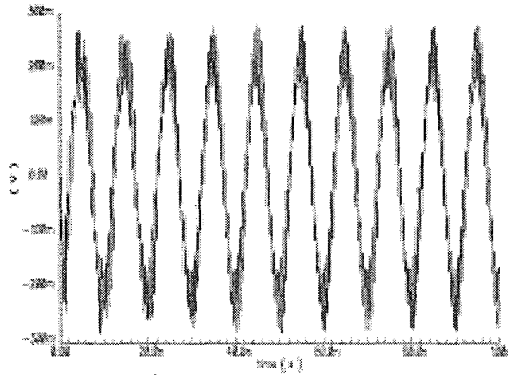

Fig. 4 – Output voltage for a 200mV 900 MHz RF input

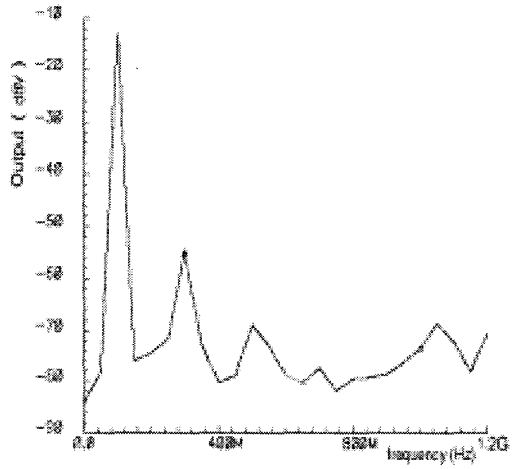

Fig. 5 – Output Spectrum

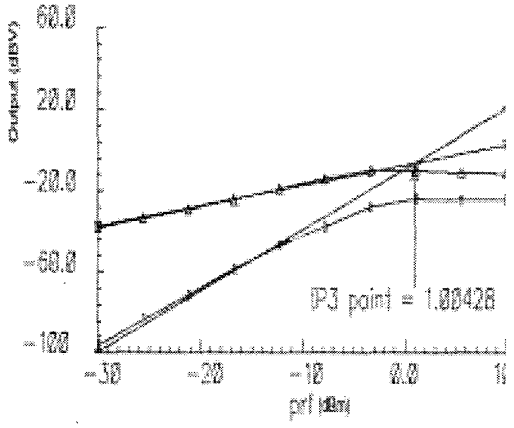

Fig. 6 – IP3 Point

4. CONCLUSION

A low-voltage CMOS mixer has been analyzed. The circuit can operate at a 1.2 V supply voltage with good simulation results. The circuit consumes 12 mW and has good linearity. Simulation results indicate that the third harmonic component lies 44 dB below the fundamental, and the circuit has an input referred IP3 of 1 dBm. The main advantage of this structure is its low-voltage operation while maintaining good linearity. The proposed structure is symmetric and occupies a small chip area making it a very feasible analog multiplier in various communication systems.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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