Layout Level Design for Testability Strategy Applied to a CMOS Cell Library

F.C. Blom(1), J. Oliver(2), M. Rullán(2), C. Ferrer(2)

(1) University of Twente P.O. Box 217, NL-7500 AE Enschede, The Netherlands
(2) CNM(CSIC) - Univ. Autònoma de Barcelona, 08193 Bellaterra (Barcelona), Spain

Abstract

The LLDFT rules used in this work allow to avoid some hard to detect faults or even undetectable faults on a cell library by modifying the cell layout whithout changing their behaviour and achieving a good level of reliability. These rules avoid some open faults or reduce their appearance probability. The main purpose has been to apply that set of LLDFT rules on the cells of the library designed at the Centre Nacional de Microelectrònica (CNM) in order to obtain a highly testable cell library. We summarize the main results (area overhead and performance degradation) of the application of the LLDFT rules on the cells.

1: Introduction

Test generation has long been recognized to be an important part of circuit design. The hard task of testing integrated circuits is becoming even more difficult, because of the rapidly expanding production of VLSI circuits.

During fabricating of an IC, disturbances in the process and contaminants (dust particles,...) may cause an incorrect behaviour. These defects can affect multiple integrated circuits on the same wafer (global defects) or can affect a small area on a single IC (local defects or spot defects).

The following types of defects have been reported as primary causes of CMOS IC failure: bridging, open drain or source, open gate, transmission gate opens, gate oxide shorts, parasitic transistor leakage and punch through defects.

The stuck-at fault is the dominant fault model used in automatic test pattern generation (ATPG) and fault simulation but the single stuck-at model is insufficient for describing faults that may occur during the fabrication of CMOS circuits, and as consequence, testing based on the stuck-at fault model cannot achieve zero defects in CMOS ICs [1].

For this reason, it has been necessary to introduce realistic fault models: *opens* (stuck-opens, floating gates...) and *shorts* (stuck-ons, gate oxide shorts, bridgings, floating gates...) [2] which depend on the technology and on the circuit layout. We refer as realistic faults those originated by likely physical defects induced during IC manufacturing.

Analysis of realistic physical failures in digital circuits is necessary to gain an understanding of the effects of faults on the functional behaviour of the circuits, to derive efficient test sets, and to redesign circuits for improved testability.

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Once the testability problem has been identified, ways to redesign the circuit with minimal overhead have to be searched. The optimal redesign seeks to decrease costs of test generation/application as well to increase fault coverage and diagnosability.

So, in order to enhance the testability of the CMOS cell library designed at the Centre Nacional de Microelectrònica [3] we have redesigned it using basic Layout-Level Design For Testability (LLDFT) rules [4], [5] to prevent or to avoid some realistic faults.

In short, the previous work about these techniques based on LLDFT rules was presented by Galiay *et al.* [6] that explained a set of layout rules for MOS circuits. After that work, different approaches have appeared on how to attach LLDFT. In this paragraph LLDFT techniques are reviewed. These techniques are divided into two main groups: switch-level techniques and layout-level techniques:

a) switch-level techniques [7], [8], [9], [10], [11], [12] that modify the circuit at the transistor level and basically consists in adding transistors. Reddy *et al.* [7] have proposed some methods for single stuck-open faults. In 1987, Liu and McCluskey [9] added an inverter in order to avoid stuck-on and stuck-open faults. In 1991, Jayasumana *et al.* [12] added one FET to avoid stuck-open faults. This technique have some drawbacks: all add extra transistor and area to the design and most need extra control lines routed to each gate.

b) layout level techniques [13], [14], [15], [16], [4], [5] that modify the layout (do not add any control lines but require the designer to work at a low-level design representation). Zasio [13] has presented a method for gate arrays. In 1987 Koeppe [14] presented a set of layout rules to cope with stuck-opens. In the same year, Vierhaus [5] proposed a set of rules to avoid bridging faults. In 1989, Soden *et al.* [15] explained some layout modifications. In 1990, Levitt *et al.* [16] made a summary and enhanced testability at layout level. In 1991, Teixeira *et al.* [4] summarized some rules to avoid faults.

In general, all these previous works show a set of rules that must be applied on a whole design. In consequence, the designer necessary has to know all related it with testability and specifically with LLDFT.

In our work, we work with these rules and we analyze which rules are better to apply on cells of the CNM library (with CNM technology) and we obtain the consequences of their application [17].

The main advantage of applying these rules in a cell-based design process is that the new redesign of each cell has to be made only once and this work must be oriented by a test engineer. Because of our objective is to enhance the testability, we can dedicate more time for this task and so we finally obtain a more compact and elaborated design.

Otherwise, if these rules are applied in every new design, the whole circuit will need to be redesigned and this may provoke an area overhead and an increase in design time (because is better to apply these rules to a small design than a big one).

We have applied these rules to a cell basic set of the CNM library and for each one we obtain the area increase and the electric behaviour. Because of we work with a cell library (that it has a limited height) we only modify the width parameter when we apply some rules. Otherwise, when the electrical behaviour is worse, could be decided on layout what transistor width has to be changed to reach the expected electrical behaviour.

The short faults (including some floating gates) have a great appearance probability and are detectable by means of IDDq measurements that are assumed to be a good test technique to detect them [18], [19]. For example, in Figure 1 we can see a NAND gate with two kind of faults: short in transistor M2 and gate oxide short in transistor M4.

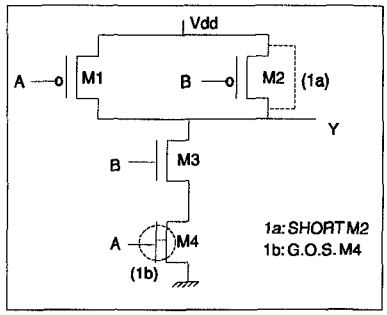

Figure 1

We can see in the Figure 2 the simulation results of the NAND without defects.

The result of simulation with a short in transistor M2 appears in Figure 3b and the result with a gate oxide short in transistor M4 is shown in Figure 3c. In both cases is remarkable a great amount of quiescent power supply current (IDDq) in comparison with the result of simulation without any defects (see Figure 3a).

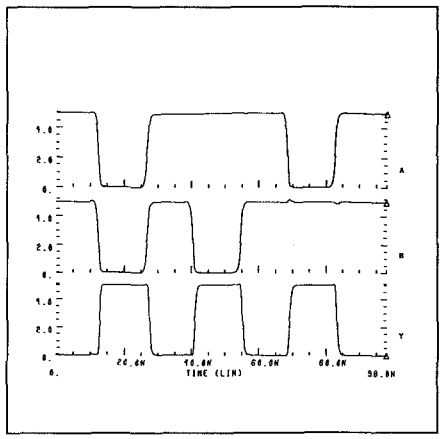

Figure 2

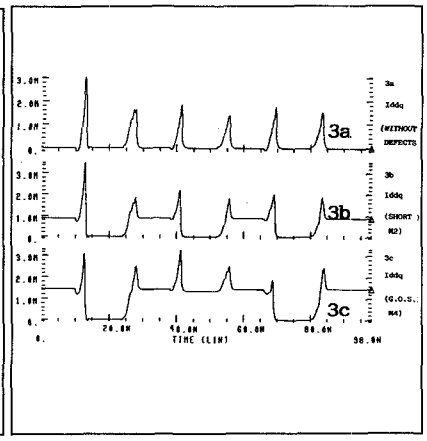

Figure 3

However, we present here the main results obtained by applying basic LLDFT rules to design out some open faults and to make the remaining opens easier to be detected.

In general, this kind of faults implies an increase of the test pattern generation cost (i.e. robust sequences, minimum test sequence composed by two vectors,...) in comparison with classical ATPG cost for stuck-at faults, and for this reason it is better to avoid them.

2: Basic LLDFT rules

To reduce the appearance probability of open faults we propose to modify the CMOS library layout using a set of LLDFT rules, because not any kind of rules can be applied on a cell library. We have chosen the following rules set :

a) Redundancy of contacts (because they have a high probability to produce opens)

b) Partial application of a ring-shaped or closed loop conductive layer [14]

We use this rule based on Koeppe with some modifications. It is not necessary to keep the transistor width in the whole ring. Some parts of the ring are just interconnecting signal lines and may have the minimum line width of the diffusion layer (in order to reduce area and diffusion resistance).

An example of a ring based on Koeppe is shown in Figure 4.

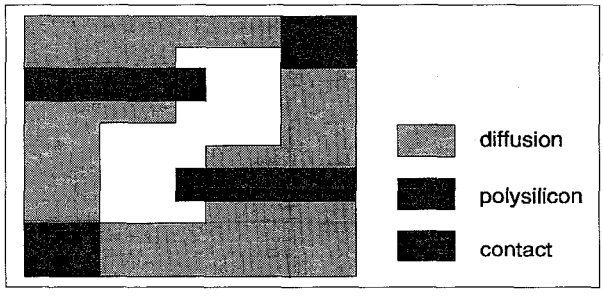

Figure 4

c) Duplication of interconnection layers and inputs (redundant conductive paths)

The previous rules are oriented to avoid open faults but, otherwise, others authors have also proposed some LLDFT rules for preventing bridging faults [4], [5], [6].

Usually, to avoid this kind of faults, the space between the adjacent conductive layers of the same material has to be increased. Many of these rules convert bridging faults in stuck-at, although the designer has difficulties for applying them (because these rules consume a lot of area and would cause a worse electrical behaviour).

In our work, we have applied in some cells the basic rule to prevent feedback bridging within a cell ("gates in larger macros should be placed according to the signal flow, in other words, avoid crossovers of input and output lines of a logical element" [4], [5]).

When possible, we apply the rule that creates lines in diffusion layers (the diffusion layer has a low probability for open faults [14]) and the interconnection of MOS transistor gates is made in polysilicon.

For example, in Figure 5 we can see a NOR cell and a redesigned cell. We have applied rule b in the pull-down path. Again, it is not necessary to keep the transistor width in the whole ring. If an open occurs in the common contact it could be detected as a stuck-at fault, and for this reason

we have only multiplied the rest of them (rule a). On the other hand we have also duplicated the input gate to avoid an open in this layer (rule c).

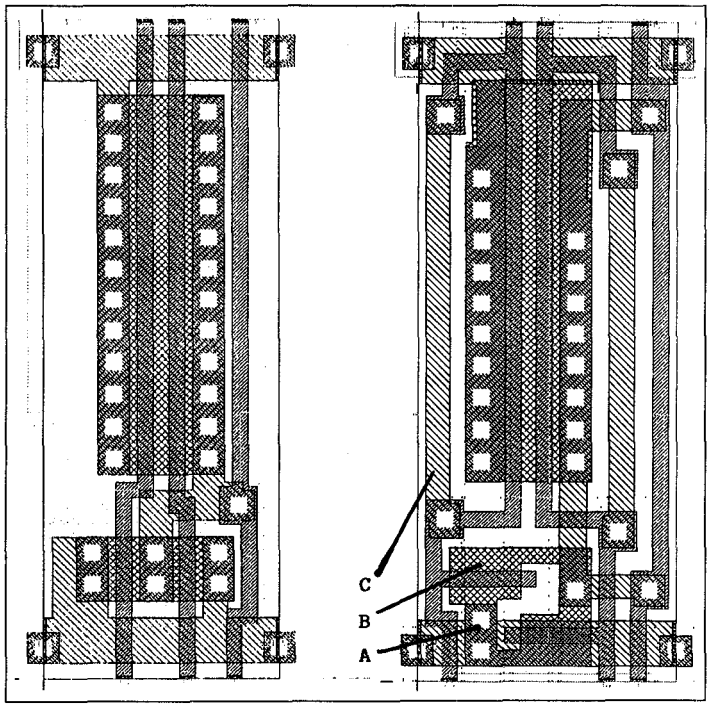

Figure 5: old and redesigned NOR cell

3: Results

Our work can be divided in two main aspects:

a) to analyze the main LLDFT rules and which of them can be applied on a cell library

b) to obtain a comparative results between old and redesigned cells.

These results have been obtained applying each time only one rule over each cell. Two important aspects of an IC have been measured in these simulations: area increase and electrical behaviour.

When a positive area increase appears, only affects to the width parameter of the cell because the height parameter is limited in all cell library.

The results shown the electrical behaviour variation (rise time, fall time, delay rise and delay fall) of the new cells compared with primitive cells. A positive percentage corresponds to an

increase in time with respect to the old cell, whereas a negative percentage corresponds to a better behaviour than the old design.

In the next tables we show the main results obtained over each cell.

NAND	RULE A (duplic. contact)	RULE B (ring of Koeppe)	RULE C (duplic. layers)
AREA %	0	6.4	31
Rise time %	0.5	44	3.7
Fall time %	0.6	-8.7	4.5
Delay rise %	1	36.7	5.3
Delay fall %	0.7	-6.2	4.3

Table NAND

NOR	RULE A (duplic. contact)	RULE B (ring of Koeppe)	RULE C (duplic. layers)
AREA %	0	5.6	0
Rise time %	0.2	0.8	1.5
Fall time %	0.4	1.8	0.6
Delay rise %	0.2	0.2	1.9
Delay fall %	0.3	-0.3	0.8

Table NOR

AND	RULE A (duplic. contacts)	RULE B (ring of Koeppe)	RULE C (duplic. layers)	RULE D (placing to signal flow)
AREA %	0	3.1	25.6	0
Rise time %	6.1	4.8	10	9.6
Fall time %	5.8	8.8	10	7.9
Delay rise %	12	14.7	26	8.5
Delay fall %	11.4	15.8	21	6.1

Table AND

OR	RULE A (duplic. contacts)	RULE B (ring of Koeppe)	RULE C (duplic. layers)	RULE D (placing to signal flow)
AREA %	0	15	36.8	0
Rise time %	5	4.6	1.3	5.6
Fall time %	4.2	10.5	2.3	4.9
Delay rise %	4.9	7.4	1.5	4.2
Delay fall %	5.7	8	-0.1	4.6

Table OR

AOI21	RULE A (duplic. contact)	RULE B (ring of Koeppe)
AREA %	0	9.9
Rise time %	1.5	3.1
Fall time %	1.9	-8.9
Delay rise %	3.1	10.2
Delay fall %	2.3	6.3

Table AOI21

AOI22	RULE A (duplic. contact)	RULE B (ring of Koeppe)
AREA %	0	4
Rise time %	1.7	2.2
Fall time %	3	3.5
Delay rise %	8.3	9.9
Delay fall %	7.2	10.5

Table AOI22

When rule C (duplication of interconnection layers) is applied we obtain the worst results because rule C causes an enormous area increase and a worse electrical behaviour. This kind of rule could only be applied when the added cost (in area or electrical behaviour) to avoid the faults occurrence was not important. Although, this rule can provoke another kind of faults (shorts between adjacent layers).

Rule A (duplication of contacts) causes an equal or slightly different electrical behaviour or area increase. For this reason there isn't any problem to apply this rule but first the designer must duplicate the important contacts (if an open faults occurs in this important contacts cause hard to detect faults or undetectable faults) and after, if there is area yet, the designer could duplicate the other contacts.

Rule B (partial application of ring based on Koeppe) depends on where the ring is placed. If the diffusion ring is placed in the pull-up part, (with a great diffusion resistance) the electrical behaviour is worse than if it was placed in the pull-down part (with a low diffusion resistance). For this reason, the electrical behaviour is better in a NOR gate than in a NAND gate.

Rule D (placing according to the signal flow) is applied to prevent feedback bridging in a cell. That is to say, to avoid crossovers of input and output lines of a logical element. This causes a worse electrical behaviour in the AND gate, but causes a good electrical behaviour in the OR gate. This rule is strongly layout dependent and it is difficult to establish an optimal criterion for use it.

4: Conclusions

In summary, in this paper we have presented the results of the LLDFT application strategy on a CMOS cell library. That presents two main advantages:

-the reduction of the faults set
-the new redesign of each cell has only to be made once

The application of these rules implies that the area overhead is always under the 10%, except when the layers and inputs (rule c) have been duplicated. The electrical behaviour is degraded around the 10% except when rule b (application of the Koeppe ring) has been applied to the AND gate.

In short, the utilization of these rules seems reasonable in order to avoid some open faults or to use easier fault models (i.e. classical stuck-at), when the new cells don't exceed the 10% of the nominal value of the primitive cells.

In a future, we want is to apply this methodology to more complex cells, to the routing area and to the ISCAS benchmark circuits. We also would want to make easier the detection of some faults (shorts, floating gate, ...) by IDDq measurements by means of the introduction of built-in current sensors in a cell-based design strategy.

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