As stable fabrication processes for microelectromechanical systems (MEMS) emerge, research efforts shift toward the design of systems of increasing complexity. Focusing on higher-level design issues is being made possible by the development of hierarchical cell design methodologies, libraries of characterized MEMS elements, mixed-technology simulators, layout synthesis tools, and design rule checking tools. By incorporating an increasing number of features and moving toward monolithic integration, MEMS are evolving from simple components to whole systems. Increased miniaturization in conjunction with an ability for mixed integration with electronic circuits are key factors for the emergence of a new generation of chips embedding MEMS. This new generation of devices offers a tremendous potential in domains as varied as the biomedicine, automotive, and telecommunications industries. MEMS are high-growth markets, and projected growth requires significant advances in computer-aided design, test, and manufacturing.1

At this early stage of development, research aspects concerning integrated design and test approaches and system validation techniques must be addressed before these chips can be moved from the laboratories to the field in a cost-effective manner. Many difficulties that can prevent the introduction of this new generation of chips are strongly related to test, including production testing costs, quality, and reliability verification. A manufactured product must be testable to ensure and prove the required quality and reliability levels. Currently, most MEMS applications correspond to low-volume niches, where functional testing is performed by adopting techniques from the test of analog electronics. The ways in which testing is going to be performed for large-volume complex devices embedding MEMS are not yet well-known, and research in this direction is just starting.2 With high safety requirements needed for most MEMS applications, achieving high quality and reliability can be addressed by the introduction of self-testing features (so far, just considered for testing of movement in accelerometers) or the use of online and fault tolerant techniques.3

The intimate linkage between form and function, a most relevant difference between MEMS and microelectronic circuits,4 stresses the need to build design models that make testing tasks, and fault injection in particular, possible. Adequate fault-free models often do not allow the injection of some types of faults, including faults caused by the most typical MEMS defects and parameter deviations.5 A structured design and test approach, based around an underlying Hardware Description Language, provides not only the

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This article illustrates how fault-based, defect-oriented test approaches can be applied to the problem of testing the next generation of chips embedding MEMS.

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best way of addressing design, validation, and test for this new generation of chips but also compatibility with standard IC practice. The structured approach leads to an adequate linkage between circuit model and physical layout, which is important for addressing tasks such as the validation of dependable systems and the generation of structured tests.

As for purely microelectronic chips, the development of cost-effective tests for large-volume chips embedding MEMS may well require test stimuli targeting actual faults, developing fault lists and fault models for realistic defects, and using fault simulation as a major approach for assessing testability and dependability. New technological steps such as silicon micromachining introduce new types of failure mechanisms and defects specific to MEMS parts. This work illustrates the integration of design and test for MEMS parts, targeting silicon micromachining defects via fault-based, defect-oriented testing as for microelectronics parts. Two classes of MEMS components are considered—suspended thermal MEMS and electrostatic micromechanical resonators—and are fabricated, respectively, by silicon bulk and surface micromachining, two of the most mature and stable MEMS technologies at present. These components can be used in wireless communication chips and thermal multifunction sensor chips, two of the domains under research where this next generation of chips can shape the future markets.

**Physical modeling and implementation**

Since the principles governing the manufacturing of MEMS are an evolution of microelectronics, superposition of different material layers is used for implementation. Mechanical, thermal, and electrical phenomena occurring in these layers are generally exploited. Examples of physical principles that are exploited in the MEMS described here are shown in Figure 1.

CMOS-compatible bulk micromachining provides a low-cost monolithic solution for the integration of MEMS. For this reason, the French Multiproject Wafer Service (known as CMP) adapted a commercial tool for the design of MEMS and provided access to these technologies. The suspended thermal MEMS concerned in this work were produced using a commercial CMOS process followed by a bulk micromachining postprocess. CMOS-compatible anisotropic etching is used to selectively remove material from the silicon substrate, giving place to membranes, cavities, masses, and bridges that are basic MEMS components for combination with microelectronics. Suspended MEMS that typically exploit thermal properties include infrared sensors, electrothermal converters, and thermal pixels.

A typical phenomenon exploited by thermal MEMS is the Seebeck effect described in Figure 1a. An electrical voltage is generated between both ends of a material when there is a temperature difference between the two ends. By joining two different materials, a thermocouple is obtained for use notably in infrared sensors. The Seebeck coefficient $\alpha$ is independent of geometrical parameters and is linked to resistivity. Thus, both material properties are affected by similar process parameters and physical failures.
Suspended parts such as bridges and membranes have a good thermal isolation from the bulk. Heat transfer can occur via the mechanisms of conduction, convection, or radiation, as shown in Figure 1b. Thermal conductances are modeled considering the geometry of the involved layers, conductivity factors ($K_i$), surface emissivity ($\varepsilon_i$, $\sigma$ is the Stephan’s constant), and environment properties such as temperature ($T_i$) and $c$-&-ling fluid (normally air natural convection, with $h_a^c$ and $h_a^c$ being the convection coefficients of the bottom and top surfaces of the beam).

The Electro-Thermal Converter (ETC) shown in Figure 2 has been fabricated by CMOS bulk micromachining. These devices are typically used as true root-mean-square converters, transferring the root-mean-square value of an AC voltage or current to its equivalent DC value. The schematic diagram of Figure 1b shows the ETC (without interface electronics) composed of a cantilever beam that supports a heating resistor at its end and a thermopile. The resistor transforms the electrical input into heat, which flows by conduction through the beam, by convection into the air surrounding the beam, and by radiation. The fact that the beam is suspended leads to an increase in thermal resistance between the resistor and the substrate (which, acting as a heat sink, corresponds to thermal ground). This increase in thermal resistance results in higher beam temperatures. The thermopile, which senses the temperature gradient and produces an output voltage, is made of a set of thermocouples connected in series. Each thermocouple is made of a couple of n- and p-type polysilicon, which have different Seebeck coefficients ($\alpha_i$). One side of each thermocouple is at thermal ground ($T_{cold}$), and the other side is near the heating resistor ($T_{hot}$), so that an electrical voltage is generated between both ends of each thermocouple when a temperature gradient $\Delta T = (T_{hot} - T_{cold})$ exists. The total voltage at the thermopile output is the number of thermocouples times the voltage through one of them. A small signal analysis of the system results in a first-order transfer function as shown in Figure 2.

Surface micromachining technologies are having increasing success in the fabrication of complex MEMS. Typically, microaccelerometers based on sensing capacitance changes and microfilters can be produced. Devices with many suspended elements, such as electrostatic comb drives and microgears for microengines, are also appearing, together with libraries of suspended elements and adequate structured-design methodologies. A sacrificial layer of a material such as silicon dioxide, polysilicon, porous silicon, or aluminum is deposited. The postprocessing operation removes this sacrificial layer to suspend the microstructure. We have used the MCNC Multiuser MEMS Processes for fabrication of microresonators. These are basically formed of a 2-μm-thick polysilicon layer deposited over a sacrificial 2-μm-thick layer of phosphosilicate glass (PSG). Contact cuts in the PSG layer allow for the formation of mechanical anchor points, which fix the microstructure to the silicon substrate. Sacrificial release is achieved by immersion of the chip in a bath of hydrofluoric acid. This wet chemical etch removes the PSG matrix that encapsulates the movable mechanical structures.

Capacitance changes, as shown in Figure 1c, are often used in accelerometers, pressure sensors, and microresonators. Seismic masses can be formed as superposition of several material layers as shown in Figure 1d. We can employ them for piezoresistive microaccelerometers and micromechanical filters, and they are characterized by their geometry—length ($L$), width ($W$), and thickness ($t$)—and mass density ($\rho_m$). A stiffness constant $k$ for a joined beam, usually composed of several layers, can be calculated from its length ($L_n$), its Young modulus ($E$), and its moment of inertia ($I$) obtained as a function of beam geometry.

Figure 3 shows a surface micromachined micromechanical resonator. MEMS resonators are being proposed for highly selective micromechanical filtering for wireless communications and high-quality factor (Q) oscillators. The resonator is a mechanical mass-spring-damper system consisting of a central shuttle mass that is suspended by two folded-beam flexures. The topology of the suspension is designed

Figure 2. CMOS-compatible silicon-bulk micromachined Electro-Thermal Converter.
to be compliant in the $x$ direction (direction of motion) and to stiffen against the orthogonal directions and torsional movement to keep the fingers of the comb-drive transducers aligned. The fundamental resonant frequency of the microresonator is given by

$$ W_o = \sqrt{\frac{k}{m}} $$

where $k$ is the system stiffness and $m$ is the effective mass of the suspended part.

The comb-drive transducers (interdigitated finger structures) are used for exciting and sensing vibration of microstructures parallel to the plane of the substrate. They are DC biased with a voltage ($V_b$) applied to the shuttle mass via the anchor points of the suspension (three pads can be seen in the resonator of Figure 3 for input, output, and DC bias). In these standard comb drives, capacitance varies linearly with displacement when the fingers of the fixed part and moving part overlap, resulting in an electrostatic driving force in the $x$ direction.

The force generated is, to the first order, independent of the position of the moving fingers and the vibration amplitude. A small-signal analysis of the microresonator behavior results in a transconductance

$$ \frac{I_o}{V_i} $$

described as a second-order band pass filtering function, centered at frequency $W_o$. Very high $Q$ values can be achieved by operating the device under a vacuum, since

$$ Q = \frac{m W_o}{c} $$

depends on the damping factor ($c$), which in turn depends on the air viscosity, which is affected by the operating pressure.

**Micromachining defects and failure mechanisms**

MEMS devices fabricated today are tested functionally. Being essentially analog devices, their test is being approached by means of techniques from the analog test domain. In general, a MEMS device must be tested as an entity after manufacturing, with all modules in interaction and after packaging. For instance, additional stresses due to packaging can significantly impact device behavior. Since encapsulation of MEMS is often a very critical issue, sometimes accounting for more than 80% of the overall cost, testing a device should also be considered before packaging, screening out defective devices as early as possible.

Functional testing of large-volume chips embedding MEMS risks being extremely expensive. As in microelectronics, the search for generating cost-effective structured tests for large-volume chips targeting realistic faults and defects is important. Research toward developing MEMS testing methodologies is just starting. For example, methodological studies for the derivation of the most common defects in surface micromachining fabrication processes are shown in Kolpekvar and Blanton. Technology process simulation with injected realistic contaminations is performed, showing that this can result in a wide variety of defective structures. In our case, the inspection of numerous monolithic CMOS-compatible bulk micromachined MEMS fabricated via the CMP service in recent years has allowed the identification of new defects and design errors that typically occur for this type of MEMS. We concentrate here on defects occurring during micromachining.

We used front-side bulk micromachining, since it allows low-cost maskless silicon etching. Areas of naked silicon exposed for micromachining are created by stacking a contact, a via, and an open in the passivation. Silicon dioxide is used for realizing the microstructures supporting the gauges of the thermal MEMS and can be combined with metal and polysilicon layers. Anisotropic etching takes place in areas of exposed silicon, creating a cavity with the shape of an inverted pyramid. The etchants used include EDP, KOH, and TMAH. EDP has the advantage that it does not significantly attack aluminum, and it does not attack passivation layers, although it is highly toxic. KOH allows very clean surfaces and etching plans, but has the disadvantage that it attacks aluminum.
TMAH has the fastest etching rate and does not attack aluminum pads when silicon or silicic acid is adequately dissolved in the solution, but pyramidal protuberances (hillocks) may appear at the bottom of the cavities created.

Figure 4a shows hillocks that appeared using a solution of 25% TMAH. Hillocks reduce the etching rate at the bottom of the cavity, and they can be a problem for thermal sensors due to thermal leakage or even prevent the release of a suspended part. Hillocks can be avoided by adding to the solution adequate quantities of peroxide.

The most common problem encountered for the fabrication of these MEMS is the presence of oxide residuals from the CMOS process in areas of naked silicon exposed for micromachining. Oxide residuals are formed from thermal silica and from different layers of oxides that are not properly cleaned during fabrication. An oxide residual can prevent the etchant from reaching the silicon underneath, thus not forming an adequate cavity. This is especially a problem for narrow regions of exposed silicon (as shown in the case of Figure 4b, where silicon was not adequately removed underneath the regions covered by the residual oxide), for regions with acute angles, or for cross-like microstructures. As a result, a microstructure may not be fully suspended, or the cavity produced may be inadequate.

Other mechanisms that can prevent a full release of a microstructure include insufficient etching time, slow etching...
rate because of an inadequate solution, and the formation
of hillocks (as shown in the microbridge of Figure 4a that
is not fully freed in its central part), or redepositions of etched
material that can occur after micromachining. In addition,
complex substances can be formed as a result of chemical
reactions that take place during silicon etching. These sub-
stances can affect the quality of the solution if stirring is not
properly done, can reduce the etching rate, or can appear
stuck on the microstructure at the end of the process.

When oxide residuals are not too thick, they often can be
eliminated by immersion of the microstructure in a hydro-
fluoric acid solution. However, hydrofluoric acid cleaning
can cause breaks or microcracks in passivation and diox-
ide layers. A silicon etchant can penetrate existing microc-
racks and cause opens in polysilicon conductors and attack
aluminum lines (in the case of KOH etching). An example
of this is shown in Figure 4c, where an inadequate passiva-
layer layer allowed KOH to penetrate and attack aluminum
lines. This can cause a catastrophic open circuit fault or pa-
rametric faults due to important deviations in circuit resistivi-
ity. For instance, some metal layers used in CMOS fabrication
are composed of aluminum together with a thin metal bar-
der layer that is not attacked by KOH. The KOH may etch
away the aluminum layer and leave the metal barrier, for
example, a thin layer of 1,000 Å of titanium tungsten. As a re-
sult, electrical conduction can occur only in this thin layer,
which results in a large increase in resistivity.

A common defect is also the attack of the etchant to alu-
minum pads, for which CMP has proposed in the past the use
of a thin layer of oxide to cover the pads to prevent the attack.
During bonding, this thin layer is broken using ultrasound.

The defects and failure mechanisms described above
have been identified in a number of test microstructures and
devices fabricated via CMP. Examples of thermal MEMS in-
clude infrared generators and sensors, electrothermal con-
verters, and thermal pixels. The CMOS fabrication processes
used are 1 µm and 0.7 µm from ATMEEL-ES2 and 1.2 µm and
0.8 µm from AMS. As an example of a failing device, Figure
4d shows an optical microscope photo of a thermal metal
chip reject. A silicon dioxide membrane is used to suspend
a polysilicon resistor. Since the beams supporting the mem-
brane have large thermal resistance, the heat generated by
the resistor results in a temperature increase in the mem-
brane and visible heat radiation. It can be observed through
the dioxide, which is semitransparent through the optical
microscope, that part of the membrane in the central part
was not freed (lighter region), and most of the heat gener-
ated by the resistor in that part is evacuated via thermal con-
duction to the bulk. The first part of the resistor is suspended,
and the heat radiation is observed.

The most typical defects that we have encountered in sur-
fase micromachined resonator test structures during mi-
cromachining include stiction of the suspended beams to
the substrate surface and the break of comb-drive fingers.
Sacrificial release of the chips shipped by MCNC is achieved
by immersion of a chip in a bath of 50% hydrofluoric acid at
room temperature for 1.5 to 2 minutes, rinsing with deion-
ized water and alcohol to reduce stiction, and drying in an
oven at 110°C for more than 10 minutes.

The largest impact on the yield of surface micromachin-
ing technologies has by far been dominated by stiction.
Stiction can occur mostly when the structure is released.
During wet chemical etching, removal of a chip from the li-
quid etchant results in a meniscus (liquid–air interface) that
often pulls suspended parts toward the substrate surface,
where they remain stuck due to capillary forces. Once in
contact, and even after the chip has dried, suspended parts
may remain stuck due to different types of adhesion forces.
For this reason, stiction can also appear during normal op-
eration due to overrange input signals or electromechani-
cal instability, which may bring the surfaces into contact
and remain stuck after the overrange voltages disappear,
resulting in impaired functionality or failure.

A movable finger placed between two fixed fingers is in an
inherently unstable position. While fingers are perfectly
aligned and centered, forces in the orthogonal direction can-
cel out. However, any small displacement in this direction
will result in unwanted lateral forces also quadratic with re-
spect to the input voltage. For an input voltage larger than a
critical voltage, side sticking may then occur. The supports
of the movable comb-drive part are designed to provide ade-
quate orthogonal direction and torsional stiffness to avoid
mechanical instabilities, allowing for movement only in the
preferred direction. However, a broken finger in a comb-driv-
e transducer may submit the shuttle to an additional torque,
depending on the position of the finger break and the num-
ber of fingers in the microstructure. These additional torques
can result in mechanical instabilities of the vibrating mass
and unwanted forces in the orthogonal direction. These forces
are at a maximum when the comb drive is at a maximum dis-
placement and can cause the folded-beam flexures to buck-
le, while the shuttle mass clamps against the alignment lines.

Hierarchical design and test

MEMS devices are most often designed using finite-ele-
m ment method (FEM) techniques or signal flow analysis. On
one hand, FEM techniques are very general, but they are ar-
duous and time consuming for system design, due to the
low level of abstraction and the lack of design hierarchy.
On the other hand, signal flow analysis does not provide a direct
linkage between physical layout and behavioral simulation
due to the high level of abstraction. Structured design of
MEMS can be achieved by means of an intermediate circuit-
level design approach. This is important for efficiency and
compatibility with standard IC design, also providing a linkage between physical layout and behavior that is required for realistic fault simulation and testing. This is illustrated here for thermal MEMS and microresonator devices.

Note first that MEMS are analog and mixed-signal devices, working at least partially in the electrical domain. Analog fault modeling generally includes two main classes of faults, according to the effect on system behavior: parametric faults, for which deviations beyond accepted tolerance of geometric layout parameters and material properties alter system performance, and catastrophic faults, for which drastic changes are present, often preventing any system utilization. This classification appears again for MEMS. What is different in the case of MEMS are new failure mechanisms and defects (introduced, for example, during micromachining) and new failure modes due to incorrect operation. By adequately modeling these fault effects for simulation, integration of design and test can be envisioned, selecting adequate test patterns that optimize defect and fault coverage and facilitate diagnosis.

Thermal MEMS are typically described using equivalent electrical circuits solved by electric simulators. We have used an analog hardware description language (HDL-A) with the underlying mixed-domain simulator ELDO. An equivalent electrical circuit model of the ETC converter in Figure 2 is given in Figure 5a, from which an HDL-A model

Figure 5. CMOS-compatible silicon-bulk micromachined electrothermal converter. (a) Equivalent electrical circuit and (b) temperature map of the cantilever beam obtained by FEM analysis for 0.5-V DC input.
can be directly obtained. The model contains four electric pins that correspond to the inputs of the heating resistor and outputs of the thermopile. The heat transfer in the microstructure is modeled by means of a one-dimensional heat transmission line. This model is validated by a coupled electrothermal FEM analysis that provides a temperature map of the cantilever beam, as shown in Figure 5b. We see that each section of the beam has approximately the same temperature. In the electrical analogy, the heating power generated in the input resistor is modeled as a current source coupled to the transmission line, where each thermal element models the thermal conductances and thermal capacitance of one beam portion. Thermal conduction, convection, and radiation losses are modeled by means of equivalent resistors. The substrate of the microstructure is treated as a heat sink at room temperature and corresponds to electrical ground.

The use of a circuit-level design approach, using several thermal elements in the transmission line, highly facilitates the injection of some of the most common faults occurring during fabrication. Figure 6a illustrates an ETC converter for which the suspended cantilever has not been fully released.

Figure 6. Fault modeling of bulk micromachining defects for thermal MEMS. (a) SEM of ETC with a cantilever only partially released during micromachining. (b) FEM simulation of faulty device. (c) Modeling of faulty behavior using a thermal short fault model in a two-dimensional heat transfer.
In this case, bulk micromachining was not applied for a sufficiently long time. It is possible to see through the silicon dioxide beam, semitransparent to the electronic microscope, the triangular shape of the silicon material under the beam that has not yet been removed. This defect changes the heat flow in the microstructure, leading to an incorrect cantilever temperature map shown by FEM analysis in Figure 6b.

The injection of this fault at the system level (see equations in Figure 2) is not possible, while the injection of this fault at device level using FEM analysis is painful. A new design model is required for each new defect. On the other hand, these defects can be conveniently modeled at circuit level using fault models such as thermal shorts. The defect in Figure 6a is modeled in Figure 6c using thermal shorts between the suspended cantilever and the substrate. A two-dimensional heat transfer model is used for the cantilever beam. As shown by the FEM analysis of Figure 6b, different temperature values exist at different nodes of each cross-section of the faulty beam as a result of the micromachining defect, and a two-dimensional model is required for accurate results. This example illustrates the fact that accurate MEMS fault simulation requires building models that can take fault injection into account as early as possible in the design process. The one-dimensional heat transfer model of Figure 5a can accurately model the fault-free device, but it does not allow for an accurate injection of faults resulting from micromachining defects. Figure 7 shows test and simulation results for the fault-free and faulty ETCs.

The response of the faulty converter to an input pulse of 1 V amplitude shows a faulty output level and a change of the system time constant. Simulation plots show the evolution of the temperature (°C) in different nodes of the beam: the higher the curve, the closer the node to the input resistor.

For the case of the microresonator, a coupled electro-
mechanical FEM analysis of the device is very difficult to perform. FEM simulations have been performed to check mechanical stress and deformations in the microstructure shuttle and the supporting folded beams. The beams must be sufficiently wide to support a maximum stress in the regions indicated in Figure 8a, given that their thickness is fixed by the fabrication process of Multiuser MEMS Processes.

Mukherjee and Fedder propose circuit-level simulation (using nodal analysis) for suspended MEMS such as microresonators. Instead of using equations that describe the global device behavior (see equations in Figure 3), circuit simulation takes into account the analysis of the interactions between basic components such as beam flexures, electrostatic gaps, plate masses, and anchors. Each component contains nodes for coupling with other components. Nodal

\textbf{Figure 8.} Surface micromachined microresonator. (a) FEM stress analysis. (b) Basic microresonator configuration. (c) ELDO simulation with 100-mV input.
simulators solve for the system’s across variables in each node (for example, position x, y, angle θ, and voltage) by making the sum of through variables in each node (forces in x and y directions, moment about θ and current) equal to zero. Component models that relate multidomain through variables in terms of across variables can be built with an HDL-A language.

As a first approach to circuit-level design, we have decomposed the device into components, including two comb-drive transducers and one mass-spring-damper system, which can have electrical and mechanical interfaces. We have used the Mentor-Graphix Framework environment adapted for MEMS for simulation with HDL-A. Figure 8b shows the schematics of the microresonator that has been placed in its simplest configuration, where a transimpedance amplifier is used at the output for current-to-voltage conversion. We used a one-dimensional (x-translation) HDL-A model for the comb-drive component. The results of AC simulation for the mechanical displacement of the shuttle and the output voltage are shown in Figure 8c. The device of Figure 3 has been designed for a central frequency of 300 kHz, with a vibration amplitude at resonance of $X_o = 0.5 \mu m$ and output current of $I_o = 100 \, nA$, for an input of $V_i = 100 \, mV$, $n = 50$ fingers in the comb drives, $V_o = 100 \, V$, and 1 MW amplifier transresistance.

The circuit-level design approach is hierarchical. In particular, the models for the comb-drive transducers should be further decomposed in order to model the most typical defects. For example, Figure 9 shows the case of the break of a comb-drive transducer finger and the decomposition of this component in basic components (beams and electrostatic gaps) for modeling the corresponding fault. A beam component is represented as an element having two nodes, including in each node three mechanical across variables (x, y, and θ) and one electrical variable (voltage). An electrostatic gap is modeled as a time-varying capacitor (electrodes can move with respect to each other). Since elements directly linked to the layout are now available, fault injection is possible. The fault corresponds to an electromechanical open that is modeled by connecting the corresponding finger to the electrical and mechanical ground rather than to the fixed arm. Lubaszewski et al. discuss techniques for fault injection in an HDL-A description. 10

As for purely microelectronics chips, the use of fault-based, defect-oriented test techniques can help the validation of complex systems and the generation of structured tests, alleviating in part high testing costs in large-volume complex devices embedding MEMS. This is illustrated here for chips that use bulk and surface silicon micromachining for the fabrication of MEMS parts. Faults caused by micromachining defects are targeted, since these are unique to the new process steps. Suspended thermal MEMS and micromechanical resonators are used as representative test vehicles, and we describe adequate fault models and simulation approaches. The effect of typical micromachining defects can be modeled using a circuit-level design approach and adequate fault models. For thermal MEMS, thermal shorts are used to model the faulty behavior caused by realistic defects. A circuit-level decomposition is also necessary to inject typical faults caused by micromachining defects such as finger breaks. In both cases, circuit design provides a structured approach that facilitates fault injection.

References


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